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SA performed research on Mixed Mode Module (MMM) technology spanning the range from applications and mixed-mode systems requirements to the baseline technologies which must be put into place to realize MMMs. SA examined promising military applications, and analyzed the critical issues relating to the design, fabricaiton, and manufacturing of MMMs for advanced electronic systems. SA has defined one such example of a system that incorporates both analog and digital components, the Global Positioning Satellite (GPS) Receiver. Strategic Analysis, Inc. also investigated the requirements for design tools for simulating an MMM with special attention paid to insuring analog and digital signal integrity and optimizing the amount of silicon or other device area on a high density MMM host substrate. SA has determined that significant effort still remains to be done in the area of CAD development for mixed signal technology so that analog and digital circuits can be simulated at the same time. The results of this research can provide direct input into the design, planning and development of next generation MMM systems for defense applications.

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Short Title:	**Research on Mixed Mode Modules**

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TABLE OF CONTENTS

1. OBJECTIVES

There is an increasing demand in today's electronics systems for greater complexity and higher performance. With data rates increasing into the 100's of MHz to multi-GHz range (X-Band), issues arise such as thermal management, reliability, miniaturization, and manufacturability which must be resolved through the development of new electronic packaging technologies. A key problem in such systems is increasing the density of the electronic components, not only to reduce size and weight, but in many cases to increase performance as well. One attractive method of accomplishing this in complex systems is multichip module (MCM) packaging technology. MCM technology permits high-density packaging of portions of high speed digital electronic systems and combined analog/digital mixed-mode functions into a Mixed Mode Module (MMM). What is required is a mixed-mode module (MMM) technology designed to provide a medium for efficiently integrating a number of technologies in high density modules with the goal of significantly impacting identified high leverage products and markets, both commercial and defense, by reducing size, weight and cost, and increasing performance. Strategic Analysis, Inc. (SA) has endeavored to achieve this goal through its Air Force program "Research On Mixed Mode Modules".

After careful evaluation and based on results achieved in this program, SA determined that additional work would be required in evaluating 3D interconnects for MMMs. SA performed analysis on interconnects for various 3D MMM architectures, and summarized the results in Progress Report #1: Research on Mixed Mode Modules, dated September 1, 1996. As a result of this effort, SA determined that research in this topic would prove of great value to the Air Force in analyzing the various architectures that are needed for 3D MMM structures. As part of Task 9 of the contract, SA determined that 3D mixed-mode systems will greatly reduce size and weight (with potential reductions of cost and significant increases in performance) for a wide range of military and commercial electronic applications.

SA also determined that further reductions can be realized in the size and weight of 3D and 2D MMMs by integrating passive components into the substrates of these modules. In some modules discrete passive devices (resistors, capacitors, inductors) can take up over 50% of the substrate area of a module. Through elimination of solder joints and reduction in the number of assembled components, this will also enable substantial improvements in the reliability of these modules for the military markets. SA proposed an additional task #10 for determining the viability of developing technologies and materials that can be used for processing passive devices into the substrates of 3D MMMs. This study also evaluated the feasibility of using these processes in current 2D MMMs. The objective of the research efforts undertaken by SA in this contract were to aid in the advancement of basic research in key areas of electronics miniaturization that may prove crucial in meeting the challenges of future Air Force warfighting.

2. STATUS OF EFFORT

SA performed research on Mixed Mode Module (MMM) technology spanning the range from applications and mixed-mode systems requirements to the baseline technologies which must be put into place to realize MMMs. SA examined promising military applications, and analyzed the critical issues relating to the design, fabrication, and manufacturing of MMMs for advanced electronic systems. SA has defined one such example of a system that incorporates both analog and digital components, the Global Positioning Satellite (GPS) Receiver. Strategic Analysis, Inc. also investigated the requirements for design tools for simulating an MMM with special attention paid to insuring analog and digital signal integrity and optimizing the amount of silicon or other device area on a high density MMM host substrate. SA has determined that significant effort still remains to be done in the area of CAD development for mixed signal technology so that analog and digital circuits can be simulated at the same time.

The ultimate packaging density of the MMM and its maximum size depend on the patterning technology. SA has evaluated some of the technological advances in cost-effective patterning and via drilling for MMM substrates. SA has also performed an analysis of various interconnect strategies for determining the architecture that would be most beneficial for MMM systems. One solution to thermal management problems resulting from high density MMMs, which SA has investigated, is to use diamond substrates which have high thermal conductivity capabilities. While the technology for MMMs is being developed, one of the things that cannot be overlooked is the integration of MMMs into systems. SA evaluated the requirements for an infrastructure to produce cost-effective MMMs. The system house responsibilities for driving the MMM technology in advanced electronic systems was analyzed. Mixed mode system packages are being produced presently, but they are not the product of well-developed design methodology. Based on careful evaluation and the results achieved in this program, SA determined that research in evaluating 3D interconnects for MMMs would prove of great value to the Air Force The principal problem that low-cost 3D electronics packaging will address is the critical need in a wide range of military systems to greatly reduce the size, weight, and volume that various vehicles and platforms must carry.

In current practice, implementing complete mixed-mode systems or sub-systems requires mounting individual packaged devices, MCMs, shielded or unshielded analog modules, and numerous passive components for filters and RF processing on a variety of substrate types. This approach constrains the size, weight and performance capabilities of defense applications. In order to meet military requirements, the development of materials and processes for integrating discrete passives (capacitors, resistors, and inductors) directly into the MMM substrate, is important since embedded passives technology can reduce substrate area by as much as ten times while providing increased performance and reliability at 1/4 of the cost. In addition, many secondary issues associated with MMM such as including cost effectiveness, yield, testability, and reliability receive little attention during the development stage of a technology, though their impact is as important as first level research questions. SA directed its research effort at the understanding the system impact of high frequency, embedded passives and

secondary issues associated with MMM technology earlier in the development cycle to more effectively direct primary research and understand applications limitations prior to instead of after project completion. Efforts focused on experimentation and microstructure analysis of early material candidates for embedded passives for high frequency applications. The results of this research can provide direct input into the design, planning and development of next generation MMM systems for defense applications.

3. ACCOMPLISHMENTS

3.1. Task One: Identify and define electronic systems that will benefit from Mixed Mode Module technology.

The portable communications and wireless market is taking advantage of Mixed Mode technology for increased functionality and performance while reducing size and costs. The military will take advantage of the new technologies for such applications as smart weapons and systems that bring real-time intelligence to the battlefield. An example of an important military application of Mixed Mode technology is the Global Positioning Systems (GPS), a worldwide satellite navigation system developed by the DoD. GPS receivers have application to both commercial and military systems and are also expected to take over the civil aviation market in the next ten years. A typical high performance GPS system using advanced MMM technology measures only about 6" x 3" x 9", consumes several watts of power, and weighs several pounds. The GPS architecture allows for partitioning into multi-use modules for a variety of requirements. A modular approach to MMMs provides savings both in NRE design costs and unit costs because of the large combined applications of the modules. MMMs also reduce the size and power of the GPS receiver to significantly increase the total GPS market potential. Using a mixed mode analog/digital module design, it is possible to reduce the overall size of the current GPS until it fits in a package the size of a wristwatch. In achieving this goal it is necessary to also incorporate the integral components such as discrete resistors, capacitors and inductors into the substrate. This technology is discussed further in Task Ten.

3.2. Task Two: Characterize the types of electronic modules suitable for integration on a Mixed Mode Module. Evaluate the suitability and level of increased performance with incorporation of optical interconnects for realizing external I/O functions.

Data transmission is increasingly the bottleneck of modern communications. In future systems, optical interconnects between and within electronic cabinets are expected to be cost effective for both commercial and military processors. Furthermore, some critical I/O bottlenecks in current embedded processors might be eliminated only by using optical interconnects. Optical I/O applications of module-level packaging include parallel and serial cabinet-to-cabinet interconnects for computer networking, workstation-to-peripheral interconnects, and commercial supercomputers. Optical interconnects using free-air or single-mode fiber optical waveguides offer extremely low dispersions. Interconnect lengths are on the order of tens of kilometers for wide signal bandwidths. With low dispersion graded-index multimode fibers, interconnect lengths are on the order of several hundreds of meters, much greater than with normal metal transmission lines. The disadvantage with this technology is the requirement for transducers at both ends. Optical transmitters and receivers are generally expensive and power consuming and add substantial signal propagation delay compared to their normal metal counterparts. The

relatively low signal amplitudes from the photodetector in the receiver must be amplified to digital signal levels with transistors of limited gain-bandwidth product which leads to significant optical receiver propagation delays. For intra-module interconnects this is a serious technical concern.

One factor that could have a profound effect on the implementation of board-level optical interconnects is the vertical-cavity surface-emitting laser (VCSEL) which has demonstrated significant performance gains and size reductions. Several VCSEL-based transceiver modules are now being offered commercially. Hewlett-Packard Co. has a 106.2-Mbit/second transceiver, packaged in a 1 x 9 configuration, as well as a Gigabit Ethernet transceiver. Vixel Corp. is bringing out a 1-Gbit/s VCSEL-based component for fiber-optic applications; and Sun Microsystems, using VCSEL technology, has put together what it calls the fastest ATM networking board available today.

Early lateral-emitting diode lasers had an awkward, 5-micron x 1,000-micron geometry. The latest VCSELs have a round aperture. In addition, the diodes radiate light vertically, making them convenient for packaging in array configurations. New devices are being manufactured with greater than 99 percent yield, and the newer oxide-contained diodes have pushed the threshold current from around 1,000 micro A to below 10 micro A. The current research goal is to push the diodes to 4 square microns and develop packaging and mounting techniques to integrate them with CMOS VLSI chips.

Another significant breakthrough is the advent of high-performance plastic fiber. Graded-index fibers made from perflourinated polymers have realized a 200-times improvement in bandwidth loss over previous plastic-fiber technology and could cut interconnect costs by a factor of 10. The high-efficiency fiber, coupled with efficient VCSELs, could reduce the power cost of interconnect at the backplane from 100 mW to around 1 mW.

3.3. Task Three: Investigate the requirements for design tools simulating a Mixed Mode Module with special attention paid to insuring analog and digital signal integrity.

Noise problems in MMMs result from the large digital signals affecting the analog circuits due to direct inductive pickup from poorly shielded signals, to the high inductance exhibited by power and ground feeds, and to the inductance in the power and ground planes from through vias, wire bonds, package leads and lead frames, and the balls in ball grid array packages. Metal layers in MMMs are too thin compared with their skin depths to shield ac magnetic fields at the near audio frequencies found in slower speed applications. Design tools that account for these effects are not available and are essential in the long run. There has been limited success in theoretically modeling the electromagnetic behavior of power and ground planes. Diagnostic test approaches to the characterization of power and ground plane noise are primitive. Such test capability will be necessary as an aid in the current "build and fix" approaches, then to test the emerging physical models, and in the long run to provide inputs to CAD development. Commercial CAD vendors have not yet focused on the mixed signal problem, due to a

lack of resources and the pressure of more immediate problems. These common CAD and measurement needs may require a cooperative, coordinated collaborative approach.

3.4. Task Four: Evaluate alternative substrate materials for Mixed Mode Module host substrate use, including extensions of PWB/MCM-L type technology to the region of higher interconnect and via densities required for Mixed Mode Modules.

As MMM circuit complexities increase, the need for heat dissipation becomes greater. MMMs with ceramic substrates offer a high thermal performance but at a high cost. This technology is used exclusively for high end niche markets. MMMs with flexible laminate substrates are a lower cost alternative, but are limited to low power commercial applications due to a high thermal resistance. SA has evaluated several technologies that offer a lower cost alternative to the ceramic substrate MMM.

David Sarnoff has developed a double-sided, low temperature co-fired ceramic on metal core technology (LTCC-M). The metal core is copper/moly/copper. The advantages of this technology are that it has more thermal conductivity than a laminate board, the metal core prevents xy shrinkage of the ceramic, and fewer processing steps are required. LTCC-M involves hours rather than weeks of processing time. A custom glass bonding layer is used to attach the ceramic to the metal core during the ceramic firing process which prevents the ceramic from shrinking in the lateral plane ($<0.5 \pm 0.1\%$ versus 10-15%). The glass-ceramic has the lowest reported dielectric loss to 40 GHz. A low cost method for laser drilling seven mil feedthroughs in the metal core is used. Silver thick film conductors for vias and traces compatible with the dielectric system formulated have been developed for this technology. An ability to fabricate thin film wiring structures on LTCC-M boards has been demonstrated. A cost analysis carried out for the LTCC-M technology shows it to be cost competitive with MCM-L.

AlliedSignal Electronics Technology Center has developed a chip-on-board MMM technology that enables both high circuit density and high power density at a significantly lower cost than ceramic. The substrate is Viagrad, a flexible polyimide laminate 2 mils thick which is a product of Sheldahl. Viagrad contains laser ablated, copper plated vias in a regular grid pattern spaced every 0.5 mm. The vias are used for both trace-routing and thermal conduits for heat to flow from the circuitry on top through the polyimide to a heat sink. The via structure lowers the thermal resistance of the polyimide to as low as 0.05 $C°/W/in^2$ as compared to 0.4 $C°/W/in^2$ for standard polyimide materials. Viagrad is also capable of operating at ambient temperatures in excess of 200°C without degrading. The substrate can be attached directly to a heat sink using a 3 mil thermoplastic adhesive. The heat sink not only serves as a cooling path for the electronics, but also acts as the mounting surface for the flex laminate substrate during assembly. A low stress epoxy is used to encapuslate the electrical components and provides a good moisture and environmental barrier.

3.5. Task Five: Investigate large area patterning and via drilling approaches for Mixed Mode Modules.

For production quantities of Multichip Module (MCM) substrates, mechanical drilling of vias represents neither a practical nor an economic option. Prices for drill bits smaller than 250 μm (10 mil) in diameter range up to $15 each - with a realistic maximum number of hits between 500 and 1000. Hit rates of less than one hole/sec and drill breakages translate into very slow processing and low yields. Reactive ion etching (RIE) presents a possible alternative. RIE generates heat, however, which can cause dimensional stability problems, and has limited spatial resolution. Wet photochemistry methods have also been investigated, but the approach has not proven economically viable, it is a low-yield (high-cost) process. IC stepper technology could be considered for via-drilling, but is not viable for low-cost MCM substrates.

A laser beam, on the other hand, is a noncontacting (i.e., zero-wear) tool that can directly drill up to hundreds of vias each second. The unique properties of lasers make them ideal tools for micromachining a wide range of materials. Lasers have been used in the semiconductor industry for a variety of tasks including photolithography and package welding. Intense laser light can be focused to a small spot (a few microns or less), so that large amounts of energy can be applied to precise locations, allowing materials to be drilled, cut, scribed, annealed, or welded. The specific interaction between a laser beam and a processed material depends on the characteristics of the material and the wavelength of the laser. Visible and infrared laser beams, such as those from Nd: YAG (1.06 μm) and CO_2 lasers (wavelength of 10.6 μm), can provide intense local heating. Targeted material is essentially boiled off or vaporized. Unfortunately, the intense heating often causes thermal damage to surrounding material. The extent of the damage is defined by the "heat affected zone" (HAZ). The output of a Nd:YAG laser can be frequency quadrupled to the deep UV (266 nm); but that process is not efficient, and the lower-power beam cannot support practical throughput rates.

With ultraviolet lasers, the process is quite different. When a UV photon is absorbed by a material such as polyimide, its energy is not converted into vibrations of the polyimide molecules (i.e., heat). Instead, it directly excites the electrons forming the molecular bonds that hold the material together. Material is thus atomized in a process called ablation. This instant (cold) process produces clean edges and little or no HAZ even in very delicate materials. The most powerful commercially available UV lasers are called excimer lasers. An excimer laser is well-suited to precision tasks, such as drilling via sites. A high-voltage discharge generates pulsed laser light from a mixture of inert gas (helium or neon mixed with argon, krypton, or xenon) and a halogen gas (fluorine or hydrogen chloride). A typical industrial excimer laser produces pulse energies of 500 mJ, with pulse durations of only 10-40 nsec. A rapid stream of such high energy pulses is ideal for percussive drilling applications. The laser "pecks" through the material at a constant rate, and hole depth can be precisely controlled by the number of pulses delivered. An excimer laser allows fast drilling because it delivers repetition rates up to 500 Hz with overall (time averaged) output powers as high as 200 W. The most widely used wavelengths are 193, 248, 308, and 351 nm. The energy density required to ablate polyimide and other polymers with 308-nm light is 300 mJ/cm^2, while gold and copper

require nearly 5 J/cm^2 for ablation. Thus, with the power level at the work surface set to around 500 mJ/cm^2, holes can be drilled completely through the polyimide (down to the pads and ground planes) without any risk of damage to the conductors.

Masks for polymer substrate drilling are either dielectric or chrome patterned on quartz. They absorb or reflect the laser beam, except at the hole locations. Excimer lasers have a finite operating cost per photon; so the wasted laser light translates directly into increased processing costs. Also, while a given laser has a maximum output power, the light fluence reaching the surface of the parts largely determines the maximum throughput. Wasted laser light raises both the fixed and variable production costs. Companies are beginning to use holographic masks and micromachined Fresnel-zone plate lenses as a viable alternative to conventional masks for substrate machining. Holographic masks are already well-proven for micromachining on a much smaller scale in microlithography for integrated circuits. They have an optical efficiency greater than 80%, since they redirect the unwanted light to the desired locations instead of blocking it. Use of holographic masks will produce much higher throughputs. Processing speed depends on the substrate thickness and the laser power. With 50 μm polyimide, users report that current masking technology allows a 25 x 25-mm area to be processed in about 10 sec. Cost depends on substrate complexity and thickness, but, for a 25 x 25 x 50 μm polyimide, the cost to drill the vias ranges from less than a cent to 3-4 cents/substrate. Holographic masks will decrease those costs by a factor of about five.

3.6. Task Six: Define and compare alternative interconnect approaches for Mixed Mode Modules.

SA has examined the capabilities of normal metal electronic interconnects in meeting requirements for 2-D and 3-D MMM applications. Electrical interconnects greatly reduce requirements for transducers or signal conditioning electronics at either the drive or receiver end and therefore offer minimal excess signal propagation delays when compared to the current state of other approaches. Normal (non-superconducting) metal interconnects are easily fabricated in high densities at low cost using chemical processes in MCM, IC or PWB processes. The principal disadvantage of normal metal interconnects is that at high frequencies the signal losses increase. Reducing the conductor size to achieve the high interconnect densities required for MMMs results in a sharp increase in the signal losses per unit length. Severe signal loss and distortion result when ohmic line resistances are not small in comparison to the characteristic impedance. Copper conductor sizes for MMM type line lengths (1" to 1 foot) are in the 10 μm to 30 μm range.

HTSC materials avoid the ohmic resistance problem since superconductors have no measurable dc resistance and surface resistance values that are negligibly small at most frequencies for digital systems. Conductor sizes of 1.5 μm to 3 μm suffice for HTSC interconnects which makes it possible to achieve extremely high interconnect densities in 2-D MMMs. HTSC have frequency-independent penetration depth and do not show the frequency dependent impedance and dispersion effects seen in normal metal lines. HTSC

materials also offer good metal shielding and ground path conductivity which results in very low crosstalk with proper conductor geometries. HTSC interconnects can be used for long, extremely wide bandwidth interconnects as well as short intra-MMM interconnects. The principal disadvantage is the need for cryogenic cooling to approximately 80°K and the lack of mature low-cost fabrication process for manufacturing high-density multi-layer HTSC interconnects.

Optical interconnects using free-air or single-mode fiber optical waveguides offer extremely low dispersions. Interconnect lengths are on the order of tens of kilometers for wide signal bandwidths. With low dispersion graded-index multimode fibers, interconnect lengths are on the order of several hundreds of meters, much greater than with normal metal transmission lines. The disadvantage with this technology is the requirement for transducers at both ends. Optical transmitters and receivers are generally expensive and power consuming and add substantial signal propagation delay compared to their normal metal counterparts. The relatively low signal amplitudes from the photodetector in the receiver must be amplified to digital signal levels with transistors of limited gain-bandwidth product which leads to significant optical receiver propagation delays. For intra-module interconnects this is a serious technical concern.

3.7. Task Seven: Research and evaluate thermal management concepts that achieve practical heat extraction from high density Mixed Mode Modules.

A key problem in implementing a high density MMM structure is developing methods for removing the heat from the cube. One way to extract heat convectively from an interconnected MMM package is to use an electrically insulating super high thermal conductivity substrate material (like diamond) to conduct the heat out laterally through the substrate material to heat sinks at opposing faces. Artificial diamond substrates produced by state of the art chemical vapor deposition (CVD) techniques, have an extremely high thermal conductivity (700-1700 W/m°C) and exhibit electrical insulating characteristics. Diamond also possesses a low coefficient of thermal expansion (CTE) (1.5 ppm/°C) which is close to the CTE value of Silicon (2.6 ppm/°C). Using diamond as substrates to conduct the heat out of the MMM structure frees the designer to fully utilize all of the space between modules to implement a high area density array of vertical interconnects between all adjacent modules in the stack to minimize interconnect delays.

One approach that SA has evaluated uses 1mm thick synthetic diamond substrates with VLSI chips bonded to their upper surface and a high-density multi-layer Cu/BCB or Cu/Polyimide X-Y interconnect mat on the bottom side. A large number (on the order of 10,000) of 4 mil diameter vias are laser-drilled through the substrate and metallized for passing signals from the chips to the controlled impedance X-Y interconnect in the bottom. 20 mil diameter fuzz buttons are retained in the spacer boards between the diamond substrates. SA has determined that as long as the vertical, Z interconnects and the horizontal, X-Y MMM interconnects have the same characteristic impedance, mixed vertical-horizontal runs should cause no signal integrity problem for implementing a 3-D diamond cube MMM.

Thermal conduction models for both (MMM-L) and additive MMMs (MMM-D), using diamond as the thermal management substrate, have been completed. These models assess the feasibility of conducting heat laterally through the diamond substrates to heat sinks located at the board edges. This frees the systems designer to fully use all of the active area of the populated substrate to implement a high density array of vertical interconnects. These models have illustrated that up to 500 watts can be dissipated from a typical 10 cm x 10 cm diamond MMM (while maintaining a viable chip junction temperature) by using forced liquid convection technology or even an advanced phase-change heat exchange approach such as spray cooling. Demonstration MMM brassboards interfaced with these selected board-edge coolers are being developed to experimentally verify these thermal modeling results.

Coupled with their silicon-matched bonding properties and electrical insulator characteristics, artificial diamond substrates are an enabling material technology for implementing extremely high density microelectronics packaging. Signal latency can be reduced by a factor of 3 over conventional 2-D MMMs through the use of an area array interconnected 3-D configuration. Applications vary from supercomputers through mainframes and high performance workstations. The technical benefits of this technology include: (1) minimization of interconnect delays in supercomputers operating above 500 MHz, (2) enhancing inter-processor I/O bandwidths in MPPs and scaleable processors, and (3) providing for resource additions to workstations such as vector and graphics processors. From a military standpoint, this technology can lead to new operational capabilities in signal and image reconnaissance systems. From a commercial viewpoint, this technology may accelerate supercomputer and various other computer product developments approaching TERAOPS performance capability.

3.8. Task Eight: Analyze the system house responsibility for driving MMM technology in advanced electronic systems.

There is currently ongoing research by the Government, Universities and industry in the area of Mixed Mode Modules. The significant advantages that MMM technology offers in size, cost and performance lend it to being integrated into high performance systems. Mixed Mode systems are becoming increasingly important in the electronics industry with increased reliance on analog sensors combined with ADCs and digital signal processing or control. Electronic packaging will have to be available to support these systems. Lowest assembly cost, lowest size/weight and highest performance all dictate use of mixed mode modules. Examples of military and commercial systems include wireless communication, global positioning systems, tactical information assistants, electronic warfare systems, automotive collision avoidance systems and smart sensors of various kinds.

Mixed mode system packages are being produced presently, but it is not the product of well developed design methodology. Unfortunately the lack of a cohesive infrastructure is hindering the integration of MMMs into high volume, viable systems.

There is a need for coordination among the developers and the users of this technology to ensure that the passive components, optimized materials, low cost manufacturing techniques and more general CAD tools being developed will in fact meet the particular needs of mixed mode systems. One of the major issues for developing MMMs will be a determination of who is responsible for integrating all of the parts onto one substrate. The device designers are only familiar with their particular technology, and the substrate manufacturers are concerned with producing only that part of the MMM. The system houses will drive the rest of the MMM infrastructure. System designers who are responsible for integrating all of the devices on an MMM substrate will need to become familiar with this technology before the pieces are in place. This technology is in the early stages of development, but one of the key considerations in its progress is to avoid the problem of integrating too many devices together on one MMM host substrate. The more integration, the narrower the market for the MMM module due to higher NRE costs and a longer learning curve.

3.9. Task Nine: Evaluate various architectures for 3D MMM structures.

The following is a summary of the benefits that 3D packaging would bring to military systems and outlines how additional effort in this area could make low-cost 3D electronics a practical reality for both military and commercial applications. The principal problem that low-cost 3-D electronics packaging will address is the critical need in a wide range of military systems to greatly reduce the size, weight, and volume that various vehicles and platforms must carry. This need is particularly obvious in the case of aircraft, manned and unmanned, but applies equally well to platforms and vehicles all across the military. A reasonable goal for 3D electronics by the year 1999 would be the capability to shrink electronics for various military applications by at least 20x in volume and 20x in weight in comparison to conventional packaging such as VME cards. The size reduction will also substantially reduce the average signal wire length and therefore cause a reduction in the digital output drive power requirements from the IC chips.

IC devices are virtually two-dimensional, and when spread in a single plane begin to cover substantial areas which leads to longer wire length, increased latency and increased output power drive. In 3-D packaging a very small (~2mm) vertical stacking pitch between boards is achieved by mounting the bare die on thin MCM-type substrates and mounting these substrates as close together as the height of the die will allow. The result is a "cube" type of form factor, which has a small size and a convenient shape, and because of the low overall dimensions, tends to offer a very low weight overhead. Interconnections between the boards are implemented by means of area arrays of high density vertical interconnects. Effective use of these vertical interconnects between boards is made possible by high densities of through vias from the top to the bottom sides of the various MMM boards making up the 3D stack. The results of this 3D electronics packaging approach is improvement in size, weight, volume, power, signal delay and bandwidths which translates into better system performance. One inherent problem which results from the high volume density of chips is that 3-D electronics packaging represents a serious challenge in thermal management. Though some promising

technologies are available (e.g., diamond substrates as a means of distributing the heat), this is an area that will require further investigation.

In the 3-D MMM packaging concept that SA evaluated, double rows of IC chips are flip-chip mounted to the MMM substrate. In between these double rows are patches of high density area interconnect pads which contact the inter-board Z-interconnect media. While one approach to thermal management is to use diamond substrate MMMs, the arrangement of the IC die, and vertical interconnects into rows allows for alternative methods of thermal management. Through-the-bulk spray cooling down the chip rows (between Z-interconnect areas) could be used as could thin cold plates sandwiched between the backs of chips and the adjacent boards with cutouts for the Z-interconnects. It is important to note that in general, the spray cooling requirements for the 3-D MMMs will be substantially lower than for conventional packaging cooling. Because of the shorter interconnect lengths in 3-D MMM packaging, the output drive power requirements of the IC chips is reduced by >2x over conventional 2-D packaging. The very small fluid volumes in spray cooling lead to very low pump power requirements. Liquid spray cooling can reduce the cooling weight and size for a 3-D MMM by 16:1.

Another critical area, besides thermal management, is the development of high density, low cost Z-interconnects. What is required is a combination of high compliance, with uniform, reliable low electrical contact resistances. The compliance can be achieved by making the conductors out of polymer fibers, with only a thin metal coating around the body of the fibers. The fibers would be suspended in a sort of random pattern in an elastomer matrix. The fiber matrix could be sliced (perpendicular to the fiber direction) in ~1 mm thick sheets. The protruding ends of the polymer fibers would be metallized and nickel plated. In order to achieve reliable low metal-to-metal contact resistance, even when the mating force between the fiber ends and the mating metal pads on the boards is low, particle interconnects are used on the fiber ends. Very tiny diamond particles are incorporated in the plated metal on the fiber ends to achieve the penetration of the surface oxide layers on the mating metal pads. Because of the large density of the Z interconnect fibers within the matrix, the medium would not have to be aligned to the mating pads on the two boards being mated, and therefore there is no need to customize the inter-layer interconnect media to the particular pad pattern on the boards being mated. This interconnection approach is an inexpensive, high volume commodity.

3.10. Task Ten: Evaluate various technologies and processes that can be used to integrate passive devices into Mixed Mode Modules.

In current practice, implementing complete mixed-mode systems or sub-systems requires mounting individual packaged devices, MCMs, shielded or unshielded analog modules, and numerous passive components for filters and RF processing on a variety of substrate types. This approach constrains the size, weight and performance capabilities of defense applications. In order to meet military requirements, the development of

materials and processes for integrating discrete passives (capacitors, resistors, and inductors) directly into the MMM substrate, is important since embedded passives technology can reduce substrate area by as much as ten times while providing increased performance and reliability at 1/4 of the cost. In addition, many secondary issues associated with MMMs such as cost effectiveness, yield, testability, and reliability receive little attention during the development stage of a technology, though their impact is as important as first level research questions.

A number of DARPA programs have focused on technologies for the implementation of mixed-signal MCMs. Mixed-signal MCM technology is understood to be one in which most of the passive components can be fabricated on the MCM substrate itself. The advantages include reduced cost and much higher densities than conventional surface mount technologies can provide. The current focus in mixed-signal MCMs is for mixed RF/digital circuitry. The first-order focus on MCM embedded resistor and capacitor test structures is on evaluating the layer properties (sheet resistance or C/A), since it is easy to calculate the resistance of embedded resistors from the sheet resistance and the capacitiance of embedded capacitors from the C/A of the dielectric layer. The characteristics of inductors is deducible from known materials characteristics and known physics (Maxwell's equations), but figuring out the inductance, let alone Q(f) for an embedded inductor is not at all simple. The quantitative details of how a bent piece of wire turns into an inductor is still pretty much a mystery. Appendix A provides more detail on how to design/analyze MCM embedded inductors, including meeting MCM inductor design goals efficiently and quickly.

4. PERSONNEL SUPPORTED

Associate - 4955.5 hours
Scientist/Engineer - 3487.5 hours
Sr. Scient/Engin II - 627 hours

5. PUBLICATIONS: NONE

6. INTERACTIONS/TRANSITIONS

6.1. Participation at Meetings, Conferences, Seminars

DARPA Electronic Packaging and Interconnect Review Meeting, February 28-March 3, 1995, at the Crystal Gateway Marriot in Crystal City

DARPA Electronic Packaging and Interconnect Review Meeting, March 13-14, 1996, at the Lansdowne Convention Center.

6.2. Consultative and advisory functions:

SA has provided input to DARPA Program Managers on the 3D Electronics information that is provided as part of this report. This information was used by Dr. James Murphy, Program Manger, DARPA/ETO, in a briefing to the Director of DARPA, Larry Lynn on July 7, 1995.

SA provided input to DARPA Program Managers on Embedded Passives for a workshop presentation on Embedded Passives, March 31, 1996

6.3. Transitions:

As a result of research performed under this contract on 3D interconnects, SA was able to provide input to DARPA that will lead to future technology applications using 3D electronics.

SA has also provided input to DARPA in a new program using MMMs for all-digital receivers and developing embedded passive technologies for the MMMs.

7. DISCOVERIES, INVENTIONS, PATENT DISCLOSURES: NONE

8. HONORS/AWARDS: NONE

APPENDIX A

Importance of Inductors in Mixed Signal MCMs

Importance of Inductors in Mixed-Signal MCMs

A number of DARPA programs are focused on technologies for the implementation of mixed-signal MCMs. The MCM-L consortium (Dr. Frank Patten and Dr. Robert Parker) has as its initial target product an rf pocket pager product which mixes rf circuitry with digital signal processing chips. Dr. James Murphy has a new mixed-signal foundry program focused on having mixed-signal MCM capabilities commercially available in the high-density MCM-D technology for both military and commercial applications. Additionally, Frank Patten's high-temperature superconductor technologies are aimed principally at high-density rf/microwave or mixed-signal applications.

Mixed-signal MCM technology is understood to be one in which most of the myriad of passive components (resistors, capacitors and inductors) required in typical analog/rf designs can be fabricated on the MCM substrate itself. The advantages of doing so (as pointed out by Dr. Nick Neclario in several recent talks) are reduced cost and much higher densities than conventional "chip shooter" surface mount technology (SMT) can provide.

In addition to the capability for the fabrication of the passive elements themselves, the most serious problems with mixed-signal MCMs is crosstalk between the high-level digital circuits and sensitive analog/rf circuitry. The most serious problem involves coupling through power supply planes, which, for best margin and highest density, necessitates having bypass capacitor planes to decouple the power planes (and correspondingly reduce the ac impedance of the power planes). This is already available in MCM-D technology; the standard nCHIP MCM processes have available 50 nF/cm^2 bypass capacitor planes, usable both for power supply bypass functions and for implementing the embedded capacitors. (Since nCHIP is the prime contractor on Jim Murphy's DARPA mixed-signal MCM foundry program, this technical issue seems under control there.) There are a number of efforts under way to bring bypass capacitor planes and effective (high capacitance per unit area [C/A]) embedded capacitor technologies to MCM-L. Within Frank Patten and Bob Parker's MCM-L consortium, there is an embedded passives effort with the University of Arkansas HiDEC facility, with RPI (Gene Rymaszewski) developing a high C/A reactively-sputtered capacitor deposition technology suitable for MCM-L. Separately, Jim Murphy has a 3-M program for embedded capacitors in MCM-Ls. Hence. while a high capacitance (high C/A) embedded capacitor technology is very important for mixed-signal MCMs, this issue is being treated elsewhere, an will not be discussed further here. Similarly, suitable embedded resistor technologies, both for MCM-D and for MCM-L, are being pursued under the programs mentioned above, and elsewhere, and will not be discussed further here.

As noted above, the focus of most of the applications interest, both military and commercial, in mixed-signal MCMs is for mixed rf/digital circuitry, with rf

frequencies up to about 1.9 GHz of principal interest. A typical characteristic of rf circuit design (as compared to baseband analog designs) is that the operating rf or if frequencies, f_S, are typically much larger than the signal bandwidths, Δf_S. Whereas in baseband analog designs the signal frequencies are generally limited by the R-C time constant at the signal nodes, this is not the case in rf designs. For example, if the capacitance at a circuit node is C_n, and the real part of the circuit impedance at the node is R_n, then the 3dB signal frequency will be of the order of $(f_S)\text{-}3dB \approx 1/2\pi R_n C_n$. With typical device and interconnect node capacitances, baseband signal frequencies are generally limited to some tens of MHz with typical device and interconnect technologies. In rf designs, the operating frequencies, f_S, are typically far above this range, and it is the signal bandwidth, Δf_S, not f_S itself, which is subject to the R-C time constant limit cited above. This rf design "miracle" of having only the signal bandwidth, not the signal frequency itself, is made possible by the use of inductors as energy storage devices in the circuits.

The key to this rf "bandpass" circuit design is the fact that while capacitance is ubiquitous, both in the active devices themselves and in the circuit interconnects, and the capacitive susceptance, as frequency is increased, rapidly dominates the impedance of signal nodes, in fact the capacitance dissipates no energy in the circuit and generates no noise. With the proper use of inductors, for any given signal frequency, f_S, it is possible to set up an energy exchange between lossless inductors and the circuit capacitance such that the capacitive susceptance effectively disappears, with respect to both signal amplitude and noise considerations. The reason for this is that the capacitive susceptance is $+j\omega C$, as compared to $-j/\omega L$ for the inductive susceptance (or correspondingly, the impedances are $-j/\omega C$ and $+j\omega L$ respectively, where as usual, $\omega=2\pi f$). Because these have opposite signs because of the different way in which capacitors and inductors store energy, they can "cancel each other out". Because of their different frequency dependencies, however, they can cancel exactly at only a single frequency, f_S, or "adequately" within a range of frequencies within the bandwidth, Δf_S, around this center frequency.

Note that underlying the effectiveness of this rf bandpass circuit design concept is that the inductors and capacitors are energy storage devices, as opposed to energy dissipation devices (like resistors). If both inductors and capacitors are lossless, they can function perfectly in these bandpass circuit functions (from both the frequency response and circuit noise standpoints). To the extent that they dissipate a significant fraction of the energy they are supposed to be just storing, the frequency response and efficiency of the rf circuits will be compromised and thermal noise will be added to the signals. As discussed later in the "Dependence of Bandwidth, Q and Noise on R_{ac} of Inductor" section (Eqs. 33 - 46), the figure of merit for inductors and capacitors is their "quality factor" or Q, defined (Eq. 33) at a frequency f as $Q(f)=\pi$ (maximum energy stored)/(energy dissipated per cycle). For nearly-ideal rf performance, designers want Q values as high as possible.

The losses in both the energy storage materials (e.g., dielectric losses in capacitors or hysteresis losses in high permeability magnetic core materials) and in the metal conductors associated with them (IR losses) serve to limit the values of Q obtainable. In practice, because the conductor geometries associated with capacitor structures tend to be highly parallel (or very low resistance), and low loss tangent dielectric materials are available capable of giving high Q values, particularly at modest rf frequencies. The situation is much more difficult for inductors. Most of the inductors used in rf applications are "air core", meaning that the active magnetic "core" region in which most of the magnetic fields reside are either air or some other dielectric material with unity relative permeability (μ_r=1). While these materials have no hysteresis losses, rather long metal thin conductor structures are required to achieve the desired inductance, L, values. As a consequence, the ac skin-effect resistance, R_{ac}, values for the inductors tend to be substantial, and hence the Q values ($Q=\omega L/R_{ac}$ for inductors) tend to be mediocre, particularly at lower frequencies. As will be discussed later, this problem of poor inductor Q tends to be aggravated as the size of the inductor structure is reduced. Since part of the intent of mixed-signal MCM technologies is to be able to be able to increase circuit densities/reduce size by making the embedded components small (keeping the MCMs small is also a part of the cost reduction strategy), making MCM embedded inductors with satisfactory values of Q (particularly at lower rf and if frequencies) within size constraints is a challenging undertaking. However, the essential role that (reasonably) high-Q inductors play in rf circuit design makes tackling this challenge very important.

Status of Embedded Inductor Design/Analysis Capabilities

I have attended reviews of a number of the DARPA mixed-signal MCM programs (e.g., Frank Patten and Bob Parker's MCM-L embedded passives reviews, and others) and have noticed a curious characteristic which is striking similar between them. That characteristic is the highly empirical approach to the whole issue of MCM embedded inductor design and analysis, in sharp contrast to that used for embedded resistors or capacitors. In embedded resistors, everybody knows that the terminal resistance will be given as the product of the number of squares in the resistor layout tomes the sheet resistance of the resistor layer. If different sized or shaped structures are fabricated, it is understood that it is for the purpose of evaluating second-order fabrication factors like contact resistance, edge effects in resistor pattern etching, etc., not to understand how a resistor works. The same is true for capacitors. Once the capacitance per unit area, $C/A=\varepsilon_o\varepsilon_r/t_d$, has been evaluated, everyone knows what (apart from edge fringing effects) what the capacitance of a given structure will be. When different sizes or shapes are fabricated, it is for the purpose of evaluating second-order fabrication or yield characteristics, or for purposes of creating structures for evaluation of operation in different regimes of frequency, not to figure out what the capacitance will be.

While the first-order focus on MCM embedded resistor and capacitor test structures is on evaluating the basic layer properties (sheet resistance or C/A), that has not been at all the case for the embedded inductor test structures. In fact, since the basic inductor critical materials characteristics are well known (lossless μ_r=1 for the core and reasonably well known metal resistivity and thickness for conductors), there would really appear to be no need for such first-order inductor test structures at all. That is, the characteristics of the inductors should be deducible from the known materials characteristics and the known physics (Maxwell's Equations). In fact, the initial inductor test structures in these programs were done with minimal a priori knowledge of what to expect for even the inductance, let alone Q, of the fabricated embedded inductors.

The reason for this is quite simple. Whereas it is extremely simple to calculate the resistance of embedded resistors from the sheet resistance of a resistor layer, and capacitance of capacitors from the C/A of the dielectric layer, figuring out the inductance, let alone Q(f) for an embedded inductor is not at all simple. While most electrical engineers have a pretty clear quantitative grasp of how capacitors and resistors work, the quantitative details just how a bent piece of wire turns into inductance remains pretty much a mystery to most people. The analysis work described in this report was done, and the report written, to help the people who need to know just how to design/analyze MCM embedded inductors to avoid wasting a lot of time building test patterns (which, in the end, only serve to verify Maxwell's Equations) zero in on MCM inductor design goals efficiently and quickly. It should be pointed out that, because of the substantial complexity of the design/analysis process for some types of MCM embedded inductor structures (particularly planar structures, in which the conductor orientation is unfavorable, or cases when other conductors [e.g., ground planes or other circuitry] lie in proximity to the inductor structure), it is good practice to verify the inductance and Q(f) (plus relevant crosstalk, etc.) performance of the final designs with realistic test patterns which match the intended application as close as possible.

Implementation of Inductors in Mixed-Signal MCMs

The approach adopted for this work, in order to focus this effort on the real problems of mixed-signal MCM design, was to conduct frequent meetings with the engineers involved in actual mixed-signal MCM work. Because the DARPA mixed-signal MCM foundry effort is just starting, I focused most of my effort on meeting with engineers at nCHIP to evaluate both the customer requirements (passed through from inputs from their system customers) and the economic/process constraints on mixed-signal MCM-Ds. While some of the detailed focus is on MCM-D technology issues, in fact, the analyses are equally applicable to MCM-L or other technologies.

One of the key questions that came up in early discussions the choice between of the implementation of embedded inductors in planar spiral form versus nCHIP's

wirebond implementation of solenoidal inductors. Some aspects of this question, such as the much greater susceptibility of the planar spiral inductors to loss/degradation of Q due to substrate conductance if non-highly insulating were considered (and won't be discussed here), but assuming highly insulating substrates, issues of relative area requirements, performance capabilities [e.g., Q and self-resonant frequency], crosstalk, etc. between spirals and solenoids are of importance. In the meetings, it was pointed out that since all planar spirals must have their axes in the same direction (the Z-direction, assuming the MCM substrate is the X-Y plane) the crosstalk between them will be maximum. On the other hand, with a wirebond solenoid embedded inductor, the magnetic dipole axis can be oriented anywhere in the X-Y plane, so it is possible to properly orient two, even fairly closely spaced, inductors to have zero crosstalk (and probably, with some spacing constraints, to find zero crosstalk orientations for three inductors). When this was discussed in the meetings, it was noted that for this to be useful, we have to have the means to calculate the orientations that will give zero crosstalk values. I agreed and accepted the task of developing the capability to calculate the magnetic fields, etc. for these structures that allow such questions to be answered.

Another very good question that came up in the meetings involves the thickness required for the substrate metallization portion of the loops in the wirebond solenoids, or the size of the wirebond wire itself, or the related issue of how to calculate the ac conductor (skin effect) losses in these structures. The issue is that, in the idealized view of a solenoid inductor, the magnetic field is strong inside the solenoid, and essentially zero outside. If that is the case, then the high-frequency surface current on the conductors (since the surface current density must equal the tangential H-field at the surface) would be near zero on the outside of the conductor, and hence the conductor loss would be essentially twice as large as you would normally think, since only half of the periphery contributes to conduction. Also, this would mean that the substrate metal might as well be made only half as many skin depths thick as would ordinarily be specified, since the bottom side doesn't contribute to high-frequency conduction anyway. (As will be shown later, this turns out <u>not</u> to be the case.)

Another design issue relating to the wirebond solenoid MCM embedded inductors is what turn-to-turn spacing (or pitch, S, of the loops making up the solenoid) is optimum. If the pitch is very tight (S small), the magnetic coupling between loops will be tighter, improving the inductance, L, to number of turns, N, ratio, and hence the Q should be improved. However, small S also implies greater turn-to-turn capacitance, and hence lower self-resonant frequency. Also, as I suggested in the kick-off meeting for the program, the use of ribbon bonds (instead of normal round wire wirebonds) offers an ideal way to sharply reduce resistance of the inductor loops without increasing eddy current losses in the conductors (because the wide direction of the conductor is parallel to the H-field, instead of perpendicular to it as in a planar spiral). However, there will be some sacrifice in how closely the turns can be spaced using ribbon bonds, as opposed to wirebonds,

3.5. Task Five: Investigate large area patterning and via drilling approaches for Mixed Mode Modules.

For production quantities of Multichip Module (MCM) substrates, mechanical drilling of vias represents neither a practical nor an economic option. Prices for drill bits smaller than 250 μm (10 mil) in diameter range up to $15 each - with a realistic maximum number of hits between 500 and 1000. Hit rates of less than one hole/sec and drill breakages translate into very slow processing and low yields. Reactive ion etching (RIE) presents a possible alternative. RIE generates heat, however, which can cause dimensional stability problems, and has limited spatial resolution. Wet photochemistry methods have also been investigated, but the approach has not proven economically viable, it is a low-yield (high-cost) process. IC stepper technology could be considered for via-drilling, but is not viable for low-cost MCM substrates.

A laser beam, on the other hand, is a noncontacting (i.e., zero-wear) tool that can directly drill up to hundreds of vias each second. The unique properties of lasers make them ideal tools for micromachining a wide range of materials. Lasers have been used in the semiconductor industry for a variety of tasks including photolithography and package welding. Intense laser light can be focused to a small spot (a few microns or less), so that large amounts of energy can be applied to precise locations, allowing materials to be drilled, cut, scribed, annealed, or welded. The specific interaction between a laser beam and a processed material depends on the characteristics of the material and the wavelength of the laser. Visible and infrared laser beams, such as those from Nd: YAG (1.06 μm) and CO_2 lasers (wavelength of 10.6 μm), can provide intense local heating. Targeted material is essentially boiled off or vaporized. Unfortunately, the intense heating often causes thermal damage to surrounding material. The extent of the damage is defined by the "heat affected zone" (HAZ). The output of a Nd:YAG laser can be frequency quadrupled to the deep UV (266 nm); but that process is not efficient, and the lower-power beam cannot support practical throughput rates.

With ultraviolet lasers, the process is quite different. When a UV photon is absorbed by a material such as polyimide, its energy is not converted into vibrations of the polyimide molecules (i.e., heat). Instead, it directly excites the electrons forming the molecular bonds that hold the material together. Material is thus atomized in a process called ablation. This instant (cold) process produces clean edges and little or no HAZ even in very delicate materials. The most powerful commercially available UV lasers are called excimer lasers. An excimer laser is well-suited to precision tasks, such as drilling via sites. A high-voltage discharge generates pulsed laser light from a mixture of inert gas (helium or neon mixed with argon, krypton, or xenon) and a halogen gas (fluorine or hydrogen chloride). A typical industrial excimer laser produces pulse energies of 500 mJ, with pulse durations of only 10-40 nsec. A rapid stream of such high energy pulses is ideal for percussive drilling applications. The laser "pecks" through the material at a constant rate, and hole depth can be precisely controlled by the number of pulses delivered. An excimer laser allows fast drilling because it delivers repetition rates up to 500 Hz with overall (time averaged) output powers as high as 200 W. The most widely used wavelengths are 193, 248, 308, and 351 nm. The energy density required to ablate polyimide and other polymers with 308-nm light is 300 mJ/cm^2, while gold and copper

require nearly 5 J/cm^2 for ablation. Thus, with the power level at the work surface set to around 500 mJ/cm^2, holes can be drilled completely through the polyimide (down to the pads and ground planes) without any risk of damage to the conductors.

Masks for polymer substrate drilling are either dielectric or chrome patterned on quartz. They absorb or reflect the laser beam, except at the hole locations. Excimer lasers have a finite operating cost per photon; so the wasted laser light translates directly into increased processing costs. Also, while a given laser has a maximum output power, the light fluence reaching the surface of the parts largely determines the maximum throughput. Wasted laser light raises both the fixed and variable production costs. Companies are beginning to use holographic masks and micromachined Fresnel-zone plate lenses as a viable alternative to conventional masks for substrate machining. Holographic masks are already well-proven for micromachining on a much smaller scale in microlithography for integrated circuits. They have an optical efficiency greater than 80%, since they redirect the unwanted light to the desired locations instead of blocking it. Use of holographic masks will produce much higher throughputs. Processing speed depends on the substrate thickness and the laser power. With 50 μm polyimide, users report that current masking technology allows a 25 x 25-mm area to be processed in about 10 sec. Cost depends on substrate complexity and thickness, but, for a 25 x 25 x 50 μm polyimide, the cost to drill the vias ranges from less than a cent to 3-4 cents/substrate. Holographic masks will decrease those costs by a factor of about five.

3.6. Task Six: Define and compare alternative interconnect approaches for Mixed Mode Modules.

SA has examined the capabilities of normal metal electronic interconnects in meeting requirements for 2-D and 3-D MMM applications. Electrical interconnects greatly reduce requirements for transducers or signal conditioning electronics at either the drive or receiver end and therefore offer minimal excess signal propagation delays when compared to the current state of other approaches. Normal (non-superconducting) metal interconnects are easily fabricated in high densities at low cost using chemical processes in MCM, IC or PWB processes. The principal disadvantage of normal metal interconnects is that at high frequencies the signal losses increase. Reducing the conductor size to achieve the high interconnect densities required for MMMs results in a sharp increase in the signal losses per unit length. Severe signal loss and distortion result when ohmic line resistances are not small in comparison to the characteristic impedance. Copper conductor sizes for MMM type line lengths (1" to 1 foot) are in the 10 μm to 30 μm range.

HTSC materials avoid the ohmic resistance problem since superconductors have no measurable dc resistance and surface resistance values that are negligibly small at most frequencies for digital systems. Conductor sizes of 1.5 μm to 3 μm suffice for HTSC interconnects which makes it possible to achieve extremely high interconnect densities in 2-D MMMs. HTSC have frequency-independent penetration depth and do not show the frequency dependent impedance and dispersion effects seen in normal metal lines. HTSC

materials also offer good metal shielding and ground path conductivity which results in very low crosstalk with proper conductor geometries. HTSC interconnects can be used for long, extremely wide bandwidth interconnects as well as short intra-MMM interconnects. The principal disadvantage is the need for cryogenic cooling to approximately 80°K and the lack of mature low-cost fabrication process for manufacturing high-density multi-layer HTSC interconnects.

Optical interconnects using free-air or single-mode fiber optical waveguides offer extremely low dispersions. Interconnect lengths are on the order of tens of kilometers for wide signal bandwidths. With low dispersion graded-index multimode fibers, interconnect lengths are on the order of several hundreds of meters, much greater than with normal metal transmission lines. The disadvantage with this technology is the requirement for transducers at both ends. Optical transmitters and receivers are generally expensive and power consuming and add substantial signal propagation delay compared to their normal metal counterparts. The relatively low signal amplitudes from the photodetector in the receiver must be amplified to digital signal levels with transistors of limited gain-bandwidth product which leads to significant optical receiver propagation delays. For intra-module interconnects this is a serious technical concern.

3.7. Task Seven: Research and evaluate thermal management concepts that achieve practical heat extraction from high density Mixed Mode Modules.

A key problem in implementing a high density MMM structure is developing methods for removing the heat from the cube. One way to extract heat convectively from an interconnected MMM package is to use an electrically insulating super high thermal conductivity substrate material (like diamond) to conduct the heat out laterally through the substrate material to heat sinks at opposing faces. Artificial diamond substrates produced by state of the art chemical vapor deposition (CVD) techniques, have an extremely high thermal conductivity (700-1700 W/m°C) and exhibit electrical insulating characteristics. Diamond also possesses a low coefficient of thermal expansion (CTE) (1.5 ppm/°C) which is close to the CTE value of Silicon (2.6 ppm/°C). Using diamond as substrates to conduct the heat out of the MMM structure frees the designer to fully utilize all of the space between modules to implement a high area density array of vertical interconnects between all adjacent modules in the stack to minimize interconnect delays.

One approach that SA has evaluated uses 1mm thick synthetic diamond substrates with VLSI chips bonded to their upper surface and a high-density multi-layer Cu/BCB or Cu/Polyimide X-Y interconnect mat on the bottom side. A large number (on the order of 10,000) of 4 mil diameter vias are laser-drilled through the substrate and metallized for passing signals from the chips to the controlled impedance X-Y interconnect in the bottom. 20 mil diameter fuzz buttons are retained in the spacer boards between the diamond substrates. SA has determined that as long as the vertical, Z interconnects and the horizontal, X-Y MMM interconnects have the same characteristic impedance, mixed vertical-horizontal runs should cause no signal integrity problem for implementing a 3-D diamond cube MMM.

Thermal conduction models for both (MMM-L) and additive MMMs (MMM-D), using diamond as the thermal management substrate, have been completed. These models assess the feasibility of conducting heat laterally through the diamond substrates to heat sinks located at the board edges. This frees the systems designer to fully use all of the active area of the populated substrate to implement a high density array of vertical interconnects. These models have illustrated that up to 500 watts can be dissipated from a typical 10 cm x 10 cm diamond MMM (while maintaining a viable chip junction temperature) by using forced liquid convection technology or even an advanced phase-change heat exchange approach such as spray cooling. Demonstration MMM brassboards interfaced with these selected board-edge coolers are being developed to experimentally verify these thermal modeling results.

Coupled with their silicon-matched bonding properties and electrical insulator characteristics, artificial diamond substrates are an enabling material technology for implementing extremely high density microelectronics packaging. Signal latency can be reduced by a factor of 3 over conventional 2-D MMMs through the use of an area array interconnected 3-D configuration. Applications vary from supercomputers through mainframes and high performance workstations. The technical benefits of this technology include: (1) minimization of interconnect delays in supercomputers operating above 500 MHz, (2) enhancing inter-processor I/O bandwidths in MPPs and scaleable processors, and (3) providing for resource additions to workstations such as vector and graphics processors. From a military standpoint, this technology can lead to new operational capabilities in signal and image reconnaissance systems. From a commercial viewpoint, this technology may accelerate supercomputer and various other computer product developments approaching TERAOPS performance capability.

3.8. Task Eight: Analyze the system house responsibility for driving MMM technology in advanced electronic systems.

There is currently ongoing research by the Government, Universities and industry in the area of Mixed Mode Modules. The significant advantages that MMM technology offers in size, cost and performance lend it to being integrated into high performance systems. Mixed Mode systems are becoming increasingly important in the electronics industry with increased reliance on analog sensors combined with ADCs and digital signal processing or control. Electronic packaging will have to be available to support these systems. Lowest assembly cost, lowest size/weight and highest performance all dictate use of mixed mode modules. Examples of military and commercial systems include wireless communication, global positioning systems, tactical information assistants, electronic warfare systems, automotive collision avoidance systems and smart sensors of various kinds.

Mixed mode system packages are being produced presently, but it is not the product of well developed design methodology. Unfortunately the lack of a cohesive infrastructure is hindering the integration of MMMs into high volume, viable systems.

There is a need for coordination among the developers and the users of this technology to ensure that the passive components, optimized materials, low cost manufacturing techniques and more general CAD tools being developed will in fact meet the particular needs of mixed mode systems. One of the major issues for developing MMMs will be a determination of who is responsible for integrating all of the parts onto one substrate. The device designers are only familiar with their particular technology, and the substrate manufacturers are concerned with producing only that part of the MMM. The system houses will drive the rest of the MMM infrastructure. System designers who are responsible for integrating all of the devices on an MMM substrate will need to become familiar with this technology before the pieces are in place. This technology is in the early stages of development, but one of the key considerations in its progress is to avoid the problem of integrating too many devices together on one MMM host substrate. The more integration, the narrower the market for the MMM module due to higher NRE costs and a longer learning curve.

3.9. Task Nine: Evaluate various architectures for 3D MMM structures.

The following is a summary of the benefits that 3D packaging would bring to military systems and outlines how additional effort in this area could make low-cost 3D electronics a practical reality for both military and commercial applications. The principal problem that low-cost 3-D electronics packaging will address is the critical need in a wide range of military systems to greatly reduce the size, weight, and volume that various vehicles and platforms must carry. This need is particularly obvious in the case of aircraft, manned and unmanned, but applies equally well to platforms and vehicles all across the military. A reasonable goal for 3D electronics by the year 1999 would be the capability to shrink electronics for various military applications by at least 20x in volume and 20x in weight in comparison to conventional packaging such as VME cards. The size reduction will also substantially reduce the average signal wire length and therefore cause a reduction in the digital output drive power requirements from the IC chips.

IC devices are virtually two-dimensional, and when spread in a single plane begin to cover substantial areas which leads to longer wire length, increased latency and increased output power drive. In 3-D packaging a very small (~2mm) vertical stacking pitch between boards is achieved by mounting the bare die on thin MCM-type substrates and mounting these substrates as close together as the height of the die will allow. The result is a "cube" type of form factor, which has a small size and a convenient shape, and because of the low overall dimensions, tends to offer a very low weight overhead. Interconnections between the boards are implemented by means of area arrays of high density vertical interconnects. Effective use of these vertical interconnects between boards is made possible by high densities of through vias from the top to the bottom sides of the various MMM boards making up the 3D stack. The results of this 3D electronics packaging approach is improvement in size, weight, volume, power, signal delay and bandwidths which translates into better system performance. One inherent problem which results from the high volume density of chips is that 3-D electronics packaging represents a serious challenge in thermal management. Though some promising

technologies are available (e.g., diamond substrates as a means of distributing the heat), this is an area that will require further investigation.

In the 3-D MMM packaging concept that SA evaluated, double rows of IC chips are flip-chip mounted to the MMM substrate. In between these double rows are patches of high density area interconnect pads which contact the inter-board Z-interconnect media. While one approach to thermal management is to use diamond substrate MMMs, the arrangement of the IC die, and vertical interconnects into rows allows for alternative methods of thermal management. Through-the-bulk spray cooling down the chip rows (between Z-interconnect areas) could be used as could thin cold plates sandwiched between the backs of chips and the adjacent boards with cutouts for the Z-interconnects. It is important to note that in general, the spray cooling requirements for the 3-D MMMs will be substantially lower than for conventional packaging cooling. Because of the shorter interconnect lengths in 3-D MMM packaging, the output drive power requirements of the IC chips is reduced by >2x over conventional 2-D packaging. The very small fluid volumes in spray cooling lead to very low pump power requirements. Liquid spray cooling can reduce the cooling weight and size for a 3-D MMM by 16:1.

Another critical area, besides thermal management, is the development of high density, low cost Z-interconnects. What is required is a combination of high compliance, with uniform, reliable low electrical contact resistances. The compliance can be achieved by making the conductors out of polymer fibers, with only a thin metal coating around the body of the fibers. The fibers would be suspended in a sort of random pattern in an elastomer matrix. The fiber matrix could be sliced (perpendicular to the fiber direction) in ~1 mm thick sheets. The protruding ends of the polymer fibers would be metallized and nickel plated. In order to achieve reliable low metal-to-metal contact resistance, even when the mating force between the fiber ends and the mating metal pads on the boards is low, particle interconnects are used on the fiber ends. Very tiny diamond particles are incorporated in the plated metal on the fiber ends to achieve the penetration of the surface oxide layers on the mating metal pads. Because of the large density of the Z interconnect fibers within the matrix, the medium would not have to be aligned to the mating pads on the two boards being mated, and therefore there is no need to customize the inter-layer interconnect media to the particular pad pattern on the boards being mated. This interconnection approach is an inexpensive, high volume commodity.

3.10. Task Ten: Evaluate various technologies and processes that can be used to integrate passive devices into Mixed Mode Modules.

In current practice, implementing complete mixed-mode systems or sub-systems requires mounting individual packaged devices, MCMs, shielded or unshielded analog modules, and numerous passive components for filters and RF processing on a variety of substrate types. This approach constrains the size, weight and performance capabilities of defense applications. In order to meet military requirements, the development of

materials and processes for integrating discrete passives (capacitors, resistors, and inductors) directly into the MMM substrate, is important since embedded passives technology can reduce substrate area by as much as ten times while providing increased performance and reliability at 1/4 of the cost. In addition, many secondary issues associated with MMMs such as cost effectiveness, yield, testability, and reliability receive little attention during the development stage of a technology, though their impact is as important as first level research questions.

A number of DARPA programs have focused on technologies for the implementation of mixed-signal MCMs. Mixed-signal MCM technology is understood to be one in which most of the passive components can be fabricated on the MCM substrate itself. The advantages include reduced cost and much higher densities than conventional surface mount technologies can provide. The current focus in mixed-signal MCMs is for mixed RF/digital circuitry. The first-order focus on MCM embedded resistor and capacitor test structures is on evaluating the layer properties (sheet resistance or C/A), since it is easy to calculate the resistance of embedded resistors from the sheet resistance and the capacitiance of embedded capacitors from the C/A of the dielectric layer. The characteristics of inductors is deducible from known materials characteristics and known physics (Maxwell's equations), but figuring out the inductance, let alone Q(f) for an embedded inductor is not at all simple. The quantitative details of how a bent piece of wire turns into an inductor is still pretty much a mystery. Appendix A provides more detail on how to design/analyze MCM embedded inductors, including meeting MCM inductor design goals efficiently and quickly.

4. PERSONNEL SUPPORTED

Associate - 4955.5 hours
Scientist/Engineer - 3487.5 hours
Sr. Scient/Engin II - 627 hours

5. PUBLICATIONS: NONE

6. INTERACTIONS/TRANSITIONS

6.1. Participation at Meetings, Conferences, Seminars
DARPA Electronic Packaging and Interconnect Review Meeting, February 28-March 3, 1995, at the Crystal Gateway Marriot in Crystal City

DARPA Electronic Packaging and Interconnect Review Meeting, March 13-14, 1996, at the Lansdowne Convention Center.

6.2. Consultative and advisory functions:
SA has provided input to DARPA Program Managers on the 3D Electronics information that is provided as part of this report. This information was used by Dr. James Murphy, Program Manger, DARPA/ETO, in a briefing to the Director of DARPA, Larry Lynn on July 7, 1995.

SA provided input to DARPA Program Managers on Embedded Passives for a workshop presentation on Embedded Passives, March 31, 1996

6.3. Transitions:
As a result of research performed under this contract on 3D interconnects, SA was able to provide input to DARPA that will lead to future technology applications using 3D electronics.

SA has also provided input to DARPA in a new program using MMMs for all-digital receivers and developing embedded passive technologies for the MMMs.

7. DISCOVERIES, INVENTIONS, PATENT DISCLOSURES: NONE

8. HONORS/AWARDS: NONE

APPENDIX A

Importance of Inductors in Mixed Signal MCMs

Importance of Inductors in Mixed-Signal MCMs

A number of DARPA programs are focused on technologies for the implementation of mixed-signal MCMs. The MCM-L consortium (Dr. Frank Patten and Dr. Robert Parker) has as its initial target product an rf pocket pager product which mixes rf circuitry with digital signal processing chips. Dr. James Murphy has a new mixed-signal foundry program focused on having mixed-signal MCM capabilities commercially available in the high-density MCM-D technology for both military and commercial applications. Additionally, Frank Patten's high-temperature superconductor technologies are aimed principally at high-density rf/microwave or mixed-signal applications.

Mixed-signal MCM technology is understood to be one in which most of the myriad of passive components (resistors, capacitors and inductors) required in typical analog/rf designs can be fabricated on the MCM substrate itself. The advantages of doing so (as pointed out by Dr. Nick Neclario in several recent talks) are reduced cost and much higher densities than conventional "chip shooter" surface mount technology (SMT) can provide.

In addition to the capability for the fabrication of the passive elements themselves, the most serious problems with mixed-signal MCMs is crosstalk between the high-level digital circuits and sensitive analog/rf circuitry. The most serious problem involves coupling through power supply planes, which, for best margin and highest density, necessitates having bypass capacitor planes to decouple the power planes (and correspondingly reduce the ac impedance of the power planes). This is already available in MCM-D technology; the standard nCHIP MCM processes have available 50 nF/cm^2 bypass capacitor planes, usable both for power supply bypass functions and for implementing the embedded capacitors. (Since nCHIP is the prime contractor on Jim Murphy's DARPA mixed-signal MCM foundry program, this technical issue seems under control there.) There are a number of efforts under way to bring bypass capacitor planes and effective (high capacitance per unit area [C/A]) embedded capacitor technologies to MCM-L. Within Frank Patten and Bob Parker's MCM-L consortium, there is an embedded passives effort with the University of Arkansas HiDEC facility, with RPI (Gene Rymaszewski) developing a high C/A reactively-sputtered capacitor deposition technology suitable for MCM-L. Separately, Jim Murphy has a 3-M program for embedded capacitors in MCM-Ls. Hence. while a high capacitance (high C/A) embedded capacitor technology is very important for mixed-signal MCMs, this issue is being treated elsewhere, an will not be discussed further here. Similarly, suitable embedded resistor technologies, both for MCM-D and for MCM-L, are being pursued under the programs mentioned above, and elsewhere, and will not be discussed further here.

As noted above, the focus of most of the applications interest, both military and commercial, in mixed-signal MCMs is for mixed rf/digital circuitry, with rf

frequencies up to about 1.9 GHz of principal interest. A typical characteristic of rf circuit design (as compared to baseband analog designs) is that the operating rf or if frequencies, f_S, are typically much larger than the signal bandwidths, Δf_S. Whereas in baseband analog designs the signal frequencies are generally limited by the R-C time constant at the signal nodes, this is not the case in rf designs. For example, if the capacitance at a circuit node is C_n, and the real part of the circuit impedance at the node is R_n, then the 3dB signal frequency will be of the order of $(f_S)\text{-}3dB \approx 1/2\pi R_n C_n$. With typical device and interconnect node capacitances, baseband signal frequencies are generally limited to some tens of MHz with typical device and interconnect technologies. In rf designs, the operating frequencies, f_S, are typically far above this range, and it is the signal bandwidth, Δf_S, not f_S itself, which is subject to the R-C time constant limit cited above. This rf design "miracle" of having only the signal bandwidth, not the signal frequency itself, is made possible by the use of inductors as energy storage devices in the circuits.

The key to this rf "bandpass" circuit design is the fact that while capacitance is ubiquitous, both in the active devices themselves and in the circuit interconnects, and the capacitive susceptance, as frequency is increased, rapidly dominates the impedance of signal nodes, in fact the capacitance dissipates no energy in the circuit and generates no noise. With the proper use of inductors, for any given signal frequency, f_S, it is possible to set up an energy exchange between lossless inductors and the circuit capacitance such that the capacitive susceptance effectively disappears, with respect to both signal amplitude and noise considerations. The reason for this is that the capacitive susceptance is $+j\omega C$, as compared to $-j/\omega L$ for the inductive susceptance (or correspondingly, the impedances are $-j/\omega C$ and $+j\omega L$ respectively, where as usual, $\omega=2\pi f$). Because these have opposite signs because of the different way in which capacitors and inductors store energy, they can "cancel each other out". Because of their different frequency dependencies, however, they can cancel exactly at only a single frequency, f_S, or "adequately" within a range of frequencies within the bandwidth, Δf_S, around this center frequency.

Note that underlying the effectiveness of this rf bandpass circuit design concept is that the inductors and capacitors are energy storage devices, as opposed to energy dissipation devices (like resistors). If both inductors and capacitors are lossless, they can function perfectly in these bandpass circuit functions (from both the frequency response and circuit noise standpoints). To the extent that they dissipate a significant fraction of the energy they are supposed to be just storing, the frequency response and efficiency of the rf circuits will be compromised and thermal noise will be added to the signals. As discussed later in the "Dependence of Bandwidth, Q and Noise on R_{ac} of Inductor" section (Eqs. 33 - 46), the figure of merit for inductors and capacitors is their "quality factor" or Q, defined (Eq. 33) at a frequency f as $Q(f)=\pi$ (maximum energy stored)/(energy dissipated per cycle). For nearly-ideal rf performance, designers want Q values as high as possible.

The losses in both the energy storage materials (e.g., dielectric losses in capacitors or hysteresis losses in high permeability magnetic core materials) and in the metal conductors associated with them (IR losses) serve to limit the values of Q obtainable. In practice, because the conductor geometries associated with capacitor structures tend to be highly parallel (or very low resistance), and low loss tangent dielectric materials are available capable of giving high Q values, particularly at modest rf frequencies. The situation is much more difficult for inductors. Most of the inductors used in rf applications are "air core", meaning that the active magnetic "core" region in which most of the magnetic fields reside are either air or some other dielectric material with unity relative permeability (μ_r=1). While these materials have no hysteresis losses, rather long metal thin conductor structures are required to achieve the desired inductance, L, values. As a consequence, the ac skin-effect resistance, R_{ac}, values for the inductors tend to be substantial, and hence the Q values ($Q=\omega L/R_{ac}$ for inductors) tend to be mediocre, particularly at lower frequencies. As will be discussed later, this problem of poor inductor Q tends to be aggravated as the size of the inductor structure is reduced. Since part of the intent of mixed-signal MCM technologies is to be able to be able to increase circuit densities/reduce size by making the embedded components small (keeping the MCMs small is also a part of the cost reduction strategy), making MCM embedded inductors with satisfactory values of Q (particularly at lower rf and if frequencies) within size constraints is a challenging undertaking. However, the essential role that (reasonably) high-Q inductors play in rf circuit design makes tackling this challenge very important.

Status of Embedded Inductor Design/Analysis Capabilities

I have attended reviews of a number of the DARPA mixed-signal MCM programs (e.g., Frank Patten and Bob Parker's MCM-L embedded passives reviews, and others) and have noticed a curious characteristic which is striking similar between them. That characteristic is the highly empirical approach to the whole issue of MCM embedded inductor design and analysis, in sharp contrast to that used for embedded resistors or capacitors. In embedded resistors, everybody knows that the terminal resistance will be given as the product of the number of squares in the resistor layout tomes the sheet resistance of the resistor layer. If different sized or shaped structures are fabricated, it is understood that it is for the purpose of evaluating second-order fabrication factors like contact resistance, edge effects in resistor pattern etching, etc., not to understand how a resistor works. The same is true for capacitors. Once the capacitance per unit area, $C/A=\varepsilon_o\varepsilon_r/t_d$, has been evaluated, everyone knows what (apart from edge fringing effects) what the capacitance of a given structure will be. When different sizes or shapes are fabricated, it is for the purpose of evaluating second-order fabrication or yield characteristics, or for purposes of creating structures for evaluation of operation in different regimes of frequency, not to figure out what the capacitance will be.

While the first-order focus on MCM embedded resistor and capacitor test structures is on evaluating the basic layer properties (sheet resistance or C/A), that has not been at all the case for the embedded inductor test structures. In fact, since the basic inductor critical materials characteristics are well known (lossless μ_r=1 for the core and reasonably well known metal resistivity and thickness for conductors), there would really appear to be no need for such first-order inductor test structures at all. That is, the characteristics of the inductors should be deducible from the known materials characteristics and the known physics (Maxwell's Equations). In fact, the initial inductor test structures in these programs were done with minimal a priori knowledge of what to expect for even the inductance, let alone Q, of the fabricated embedded inductors.

The reason for this is quite simple. Whereas it is extremely simple to calculate the resistance of embedded resistors from the sheet resistance of a resistor layer, and capacitance of capacitors from the C/A of the dielectric layer, figuring out the inductance, let alone Q(f) for an embedded inductor is not at all simple. While most electrical engineers have a pretty clear quantitative grasp of how capacitors and resistors work, the quantitative details just how a bent piece of wire turns into inductance remains pretty much a mystery to most people. The analysis work described in this report was done, and the report written, to help the people who need to know just how to design/analyze MCM embedded inductors to avoid wasting a lot of time building test patterns (which, in the end, only serve to verify Maxwell's Equations) zero in on MCM inductor design goals efficiently and quickly. It should be pointed out that, because of the substantial complexity of the design/analysis process for some types of MCM embedded inductor structures (particularly planar structures, in which the conductor orientation is unfavorable, or cases when other conductors [e.g., ground planes or other circuitry] lie in proximity to the inductor structure), it is good practice to verify the inductance and Q(f) (plus relevant crosstalk, etc.) performance of the final designs with realistic test patterns which match the intended application as close as possible.

Implementation of Inductors in Mixed-Signal MCMs

The approach adopted for this work, in order to focus this effort on the real problems of mixed-signal MCM design, was to conduct frequent meetings with the engineers involved in actual mixed-signal MCM work. Because the DARPA mixed-signal MCM foundry effort is just starting, I focused most of my effort on meeting with engineers at nCHIP to evaluate both the customer requirements (passed through from inputs from their system customers) and the economic/process constraints on mixed-signal MCM-Ds. While some of the detailed focus is on MCM-D technology issues, in fact, the analyses are equally applicable to MCM-L or other technologies.

One of the key questions that came up in early discussions the choice between of the implementation of embedded inductors in planar spiral form versus nCHIP's

wirebond implementation of solenoidal inductors. Some aspects of this question, such as the much greater susceptibility of the planar spiral inductors to loss/degradation of Q due to substrate conductance if non-highly insulating were considered (and won't be discussed here), but assuming highly insulating substrates, issues of relative area requirements, performance capabilities [e.g., Q and self-resonant frequency], crosstalk, etc. between spirals and solenoids are of importance. In the meetings, it was pointed out that since all planar spirals must have their axes in the same direction (the Z-direction, assuming the MCM substrate is the X-Y plane) the crosstalk between them will be maximum. On the other hand, with a wirebond solenoid embedded inductor, the magnetic dipole axis can be oriented anywhere in the X-Y plane, so it is possible to properly orient two, even fairly closely spaced, inductors to have zero crosstalk (and probably, with some spacing constraints, to find zero crosstalk orientations for three inductors). When this was discussed in the meetings, it was noted that for this to be useful, we have to have the means to calculate the orientations that will give zero crosstalk values. I agreed and accepted the task of developing the capability to calculate the magnetic fields, etc. for these structures that allow such questions to be answered.

Another very good question that came up in the meetings involves the thickness required for the substrate metallization portion of the loops in the wirebond solenoids, or the size of the wirebond wire itself, or the related issue of how to calculate the ac conductor (skin effect) losses in these structures. The issue is that, in the idealized view of a solenoid inductor, the magnetic field is strong inside the solenoid, and essentially zero outside. If that is the case, then the high-frequency surface current on the conductors (since the surface current density must equal the tangential H-field at the surface) would be near zero on the outside of the conductor, and hence the conductor loss would be essentially twice as large as you would normally think, since only half of the periphery contributes to conduction. Also, this would mean that the substrate metal might as well be made only half as many skin depths thick as would ordinarily be specified, since the bottom side doesn't contribute to high-frequency conduction anyway. (As will be shown later, this turns out <u>not</u> to be the case.)

Another design issue relating to the wirebond solenoid MCM embedded inductors is what turn-to-turn spacing (or pitch, S, of the loops making up the solenoid) is optimum. If the pitch is very tight (S small), the magnetic coupling between loops will be tighter, improving the inductance, L, to number of turns, N, ratio, and hence the Q should be improved. However, small S also implies greater turn-to-turn capacitance, and hence lower self-resonant frequency. Also, as I suggested in the kick-off meeting for the program, the use of ribbon bonds (instead of normal round wire wirebonds) offers an ideal way to sharply reduce resistance of the inductor loops without increasing eddy current losses in the conductors (because the wide direction of the conductor is parallel to the H-field, instead of perpendicular to it as in a planar spiral). However, there will be some sacrifice in how closely the turns can be spaced using ribbon bonds, as opposed to wirebonds,

and hence a detailed quantitative analysis of the effects on L and R that determine Q will be necessary to optimize Q for MCM embedded solenoid inductors.

In light of these numerous, and important, design questions about embedded inductors in mixed-signal MCMs requiring detailed quantitative answers, I took upon myself the task of coming up with analytical and numerical tools of analysis capable of dealing with both planar spiral and solenoidal embedded inductor structures. This has turned out to be quite a bit of work, but very valuable in providing exactly the kinds of insights and answers needed for the design and analysis of MCM embedded inductor structures.

Stacked or Concentric Loop Approaches to Modeling the Magnetic Fields and Inductances of Solenoidal or Spiral Embedded Inductors

There exist in handbooks innumerable empirical formulas for calculating the approximate inductance of various spiral or solenoidal inductor structures. Unfortunately, in applying such formulas the designer has limited knowledge of whether the particular formula is accurate in the range of design parameters in which he is interested, and they provide no insight at all into the type of design questions that were cited above. Further, they only serve to deepen the sense of abstruseness which seems to surround magnetic fields and inductor structures. While no designer has any problem converting bulk or sheet resistivity and geometry into resistance, or converting dielectric constant and at least simple geometries into capacitance, just how a bent wire and the permeability of free space gets turned into magnetic fields and inductance is pretty much a mystery to most designers. Since the principal purpose here is to achieve insight, as well as quantitative treatment of some fairly subtle questions about MCM embedded inductors and their implementation, I decided at the outset that the only approach which could accomplish these goals would be to start from first principles along an analysis path that is both understandable and mathematically tractable. I found the solution to both of these requirements in the recognition that both the planar spiral inductors and the solenoid inductor structures may both be viewed simply as an assemblage of coaxial circular loops.

Figure 1 shows a planar spiral inductor structure as might be used as an MCM embedded inductor. The structure is drawn in Figure 1, not as a spiral, but as collection of nested coaxial, coplanar circular loops of decreasing radii, R. It is intuitively obvious that this structure will give virtually identical inductance and H-field characteristics to a true spiral, and would probably be closer to the kind of layout that would be practically done in MCMs (actually, octagons are typically used to approximate the circles). Recognizing this, the magnetic field produced by an N-turn (N-loop) spiral can be obtained as the sum of the fields from the current, I, passing through the collection of loops, and its inductance may be obtained as the

sum of the self inductances of the N loops plus all of the combination of mutual inductances between the different loops (N^2 terms in all).

Figure 2 shows the same concept applied to the solenoid inductor case. Here, instead of treating the actual helical conductor geometry, it is intuitively obvious that (since the conductor spacings and radii are the same) the treatment as a series of stacked circular coaxial loops, all of identical radius, R, separated from one another by a stacking pitch, S, will give essentially the same fields and inductance as a helix of radius, R, and winding pitch, S. As for the spiral, the magnetic field produced by an N-turn (N-loop) solenoid at any point can be obtained by summing the magnetic fields produced by the current, I, passing through each of the loops in the stack (recognizing that each will be at a different height relative to the measurement point), and the inductance of the solenoid may be obtained as the sum of the self inductances, L_{ii}, of the N loops (which will be identical for all N loops) plus all of the combination of mutual inductances, M_{ij}, between the different loops (which will depend on the vertical separation between the pairs of loops in the stack). Again, there will be N L_{ii} terms and N(N-1) M_{ij} terms (for $i \neq j$) or N^2 total terms to be summed to give the inductance for the N-loop solenoid (because $M_{ij}=M_{ji}$, only half of these are independent, and all of the L_{ii} are the same for the solenoid [but not for the spiral]). While summing these magnetic field or mutual inductance terms does represent an increasing amount of arithmetic as the number of turns or loops, N, increases, it is inherently very simple, and the type of computation which, with proper organization, can be nicely handled in a spreadsheet (EXCEL 4.0 was used in this work).

A very nice feature of this approach of modeling MCM embedded spiral or solenoidal inductor structures as a collection of coaxial loops is that we have only one electromagnetic fields problem to solve (actually, one magnetic fields problem, since we are analyzing the low-frequency magnetic fields and inductances where the dimensions of the inductor structure are small in comparison to a wavelength). Ordinarily, the bane of E&M is that every time you want to examine a new problem, you are back to solving Maxwell's Equations for the new geometry. We have only one general magnetic field case to solve; calculating the H-field above a circular loop of radius R, at a measurement point at some height, d, above the plane of the loop and radius, r from its axis. We have only one general mutual inductance case to solve; the case of the mutual inductance between two coaxial circular loops of two different radii displaced by a vertical distance, d. Of course, for the spiral inductor, all of the loops are coplanar, but this is just the general case with d=0, so we still have only one E&M geometry to solve (and fortunately, it is not very difficult).

Calculation of the Low Frequency Magnetic Field Above a Loop

I had considered putting the details of the analysis for the calculation of the magnetic fields for the loop an appendix, but in light of the purpose of all of this to dispel the mystery surrounding inductors, that would be counterproductive to our goal. Further, the calculation is actually very simple, with very few "gory details", and the simplicity is a key part of the point, so let's just quickly walk through the process from first principles to getting plots of the magnetic field strength vs. radial position at various heights above a circular loop.

In the first place, because we are interested in the low-frequency, "static" fields (where the dimensions of the inductor structure are small in comparison to a wavelength), we don't have to cope with the simultaneous solution of Maxwell's Equations, but rather can go directly to Ampere's law for the loop geometry defined in Figure 3. We will consider only situations in which the permeability, μ, of the medium is constant and isotropic (and for the actual calculations, equal to the permeability of free space, $\mu o = 4\pi \times 10^{-7}$ henries/meter), so at any point $\mathbf{r}$ the B-field is simply given as

$$\mathbf{B}(\mathbf{r}) = \mu \mathbf{H}(\mathbf{r}) \qquad \text{Eq. 1}$$

where bold face type is used to indicate vector quantities. Because the numbers are more convenient for H-fields, the field plots will be given in terms of H-field, only converting to B-field when necessary to calculate inductance, from the B-field.

Amperes law is very simple. If a differential segment of conductor, dl, of length, dl, located at some point in space, $\mathbf{r}'$, carries a current, I, then the magnitude of the differential H-field produced at a point $\mathbf{r}$ by this current will be given by

$$dH(\mathbf{r}) = [I\, dl \sin\phi]/[4\pi |\mathbf{r} - \mathbf{r}'|^2] \qquad \text{Eq. 2}$$

where $|\mathbf{r}-\mathbf{r}'|^2$ is just the square of the distance between $\mathbf{r}$ and $\mathbf{r}'$, and $\sin\phi$ is just the sine of the angle between the vector $(\mathbf{r} - \mathbf{r}')$ and dl. The direction of $\mathbf{H}(\mathbf{r})$ is mutually perpendicular to both $(\mathbf{r} - \mathbf{r}')$ and dl. While this is all you need to solve the loop field problem, it turns out to be a lot simpler to keep the trigonometry straight if you use the cross-product vector notation, in which form Eq. 2 is expressed as

$$dH(\mathbf{r}) = [I\, dl \times (\mathbf{r} - \mathbf{r}')]/[4\pi |\mathbf{r} - \mathbf{r}'|^3] \qquad \text{Eq. 3}$$

The advantage of this notation is that it keeps all of the work very simple and easy. The disadvantage is that you have to remember the definition of the cross product, which is simply

$$\mathbf{A} \times \mathbf{B} = a_X(A_yB_Z - A_ZB_y) + a_y(A_ZB_X - A_XB_Z) + a_Z(A_XB_y - A_yB_X) \qquad \text{Eq. 4}$$

where a_x, a_y and a_z are the unit vectors in the x, y, and z directions. You can find all of this, of course, in any good E&M text (my favorite being Ramo, Whinnery and Van Duzer, "Fields and Waves in Communication Electronics", in which Sections 2.24 and 5.23 are particularly relevant here), but the point in going through this derivation is that it is simple enough that you don't need to "look it up". (I did this the first time through on the plane between Dulles and California and got it right.)

What we are looking for, as seen in Figure 3, is the total field, H(r), due to the current, I, flowing in the loop of radius, R, in the X-Y plane, having as its axis the Z axis. To get this field, H(r), we are going to have to sum all of the differential currents, dH(r) (from Eq. 3) from all of the differential conductor segments, dl, forming the loop. A convenient way to do this is to specify the position around the loop by an angle, θ, taken from the X-axis (and we pick our measurement point, r, to lie in the X-Z plane, without any loss in generality, since the loop has circular symmetry). The length of the differential conductor segment associated with a differential angle, $d\theta$, around the conductor loop will just be $dl=Rd\theta$, and the components of dl will be

$$dl_x = -R\sin\theta\, d\theta, \quad dl_y = R\cos\theta\, d\theta, \quad \text{and} \quad dl_z = 0 \qquad \text{Eq. 5}$$

The location, r', of the field-generation segment, dl, on the loop will be given by

$$r'_x = R\cos\theta, \quad r'_y = R\sin\theta \quad \text{and} \quad r'_z = 0 \qquad \text{Eq. 6}$$

If the measurement point, r, is at height z=d in the X-Z plane (y=0), at a distance r = x from the z axis, then the components of r are

$$r_x = r, \quad r_y = 0, \quad \text{and} \quad r_z = d \qquad \text{Eq. 7}$$

and the components of $(r - r')$ are

$$(r - r')_x = r - R\cos\theta, \quad (r - r')_y = -R\sin\theta, \quad \text{and} \quad (r - r')_z = d \qquad \text{Eq. 8}$$

which gives, for $|r - r'|^2$

$$\begin{aligned} |r - r'|^2 &= r^2 - 2rR\cos\theta + R^2 + d^2 \\ &= R^2[(r/R)^2 - 2(r/R)\cos\theta + 1 + (d/R)^2] \end{aligned} \qquad \text{Eq. 9}$$

where the latter form, normalizing all dimensions to R, is the most convenient. Note that for substitution as the denominator in Eq. 3, Eq. 9 must be raised to the 3/2 power.

The numerator of Eq. 3 is obtained from $dl \times (r - r')$, the axial (Z) component of which is given from Eqs. 4, 5 and 8 as

$$[dl \times (r - r')]_Z = dl_X (r - r')_Y - dl_Y (r - r')_X$$
$$= (-R \sin\theta\, d\theta)(-R \sin\theta) - (R \cos\theta\, d\theta)(r - R \cos\theta)$$
$$= R^2[1-(r/R)\cos\theta]d\theta \qquad \text{Eq. 10}$$

While the axial, Z-component of field does all of the work in the cases of interest, for nulling out the crosstalk, we also would like to know the radial (X) component of field, which we get similarly as

$$[dl \times (r - r')]_X = dl_Y (r - r')_Z - dl_Z (r - r')_Y$$
$$= (R \cos\theta\, d\theta)(d) - (0)(-R \sin\theta)$$
$$= R^2[(d/R)\cos\theta]d\theta \qquad \text{Eq. 11}$$

While there is a local differential tangential field component, dHy, for some values of q, from the circular symmetry of the ring, this component must integrate to zero, and so we need not bother with it here.

From Eqs. 10 and 11, we obtain the differential contributions to the axial, $H_Z(r,d)$ and radial $H_X(r,d)$ components of H(r), dH(r), at height d and radius r, as

$$dH_Z(r, d) = (I/4\pi R)[1-(r/R)\cos\theta]/[(r/R)^2 - 2(r/R)\cos\theta + 1 + (d/R)^2]^{3/2}d\theta \qquad \text{Eq. 12}$$

We get $H_Z(r, d)$ by integrating $dH_Z(r, d)$ around the loop (from $\theta = 0$ to 2π), which by symmetry we can simplify by just multiplying by 2 and integrating from $\theta = 0$ to π,

$$H_Z(r, d) = (I/2\pi R)\int_0^{\pi} [1-(r/R)\cos\theta]d\theta/[(r/R)^2 - 2(r/R)\cos\theta + 1 + (d/R)^2]^{3/2} \qquad \text{Eq. 13}$$

we can do the same for the radial field component, $Hr(r, d) = Hx(r, d)$ as

$$H_r(r, d) = (I/2\pi R)\,(d/R)\int_0^{\pi} \cos\theta\, d\theta/[(r/R)^2 - 2(r/R)\cos\theta + 1 + (d/R)^2]^{3/2} \qquad \text{Eq. 14}$$

While integrating Eq. 13 for $H_Z(r, d)$ analytically looks a little daunting, for the simpler case of r=0 there is no θ dependence at all, so we obtain the axial field strength, H_Z, versus height, d on the axis of the loop as

$$H_Z(r=0, d) = (I/2R)/[1 + (d/R)^2]^{3/2} \qquad \text{Eq. 15}$$

or for d=0 (in the plane of the loop, d=0, at its center, r=0),

$$H_Z(r=0, d=0) = (I/2R) \qquad \text{Eq. 16}$$

It is quite possible that there are analytical solutions to the definite integrals of Eqs. 13 and 14. (I didn't have a table of integrals on the plane, and haven't really tried hard to integrate the functions subsequently.) I know that $H_Z(r,d)$ can be expressed as the derivative of complete elliptic integral functions, but it seems a lot simpler to just numerically integrate these to get the H-field. I found it quite straightforward to just do this in an EXCEL 4.0 spreadsheet calculation. The only concern in carrying out this integral numerically is that it has a $1/r$ singularity at $r=R$ for $d=0$ (the denominator goes to zero near $\theta=0$). This is of course correct; the H-field would indeed become infinite if the conductor radius were reduced to zero. Practically, it means that the integration step size, $\Delta\theta$, must be made quite small near $\theta=0$ when r/R is near unity and d/R is near zero (e.g., near the surface of the conductor, when the radius of the conductor is small).

I have included two spreadsheet $H_Z(r, d)$ calculations which calculate, at one time, the magnetic field strengths at numerous radial distances, r, from the axis at the specified height above the loop. It is important to note that these calculations are for the external (outside the metal conductor itself) magnetic field from a circular loop fabricated with circular cross-section wire. Within the wire, at low frequencies, the H-field falls linearly to zero from the surface of the conductor to its center. At higher frequencies, the skin effect forces a more rapid fall-off of current with distance from the surface. The Macintosh filenames for the two $H_Z(r, d)$ calculation EXCEL 4.0 spreadsheets are "New Loop B-Field Calc at d" and "Expanded Loop B-Field Calc at d" (in spite of the names, they calculate H_Z values which must be multiplied by μ if you want B_Z). The larger of the two spreadsheets ("Expanded...") calculates $H_Z(r, d)$ for 75 values of radial distance, r, at the specified height, d, and uses quite a small integration step size to maintain accuracy quite near $r=R$ for $d=0$, so it is fairly large (and takes ≈30 seconds to recalculate on a Macintosh IIfx after a parameter is changed). Figures 4, 5 and 6 show plots of $H_Z(r/R, d/R)$ [in ampere-turns per meter] for 20 different heights, d/R, above an R=1 meter loop for a current of I=1 ampere in the loop (to scale for other loop sizes or currents, just divide H values by the actual loop radius, R, in meters, and multiply by the actual current, I, in amperes. As seen in Figure 4, the H-field at the center of the loop (r=0) in the plane of the loop is indeed 0.5 ampere-turns/meter, as indicated by Eq. 16. In the plane of the loop, Hz(r, d=0) is fairly flat near the center, then increases as $1/(R-r)$ near the conductor, reversing sign for $r/R>1$, with a negative, $-1/(r-R)$, singularity and drop-off with increasing r/R. As the height, d/R, is increased, the field inside the loop drops off somewhat, the dramatic increase near $r/R=1$ becomes much less pronounced or disappears (beyond $d/R=0.4$ or 0.5), with the radius at which the field direction becomes negative increasing to $r/R=1.85$ at $d/R=0.4$. Figure 5 is plotted with a ±5 ampere-turn/meter scale to show the field enhancement near $r/R=1$ better, while Figure 6 plots only the $0.9\leq r/R\leq 1.1$ region on a ±65 a-T/m scale.

Calculation of the Mutual Inductance Between Coaxial Loops at d

In order to calculate the inductances for the practical inductor structures shown in Figures 1 and 2, we need to be able to calculate the self-inductance of a loop of radius, R, and the mutual inductance between different sized coaxial loops displaced from one another by some height. As discussed in Van Duzer and other texts, there are several methods for the calculation of the mutual inductance between circuits. Since we already have the H-field (and hence the B-field after multiplying by μ), we can simply use the surface integral (Stoke' theorem) form where the mutual inductance, M_{12}, (which is the ratio of voltage induced in loop 1 to the time derivative of current in loop 2) is given as

$$M_{12} = (1/I_2)\int_{S_1} B_2 \bullet dS_1 \qquad \text{Eq. 17}$$

where the surface integral is bounded by the center of the conductor forming loop 1. Consider our case, as in Figure 3, of a fixed loop (loop 2 in Eq. 17) of radius, R_2, lying in the X-Y plane and a second loop, coaxial with the first, of radius, R_1, lying above it at a height, d. The surface integral will be conducted over the area of the disc of radius, R1, enclosed by loop 1. Since this disc is horizontal, **dS1** is vertical (pointing in the Z direction), so the only component of B-field that will contribute is $B_Z = \mu H_Z$. Hence, for some height d, all we have to do is integrate μ times the appropriate $H_Z(r, d)$ curve in Figure 4 from r=0 to r=R_1 to get M_{12}. The integral is over area, dA=r dr, of course, so we have

$$M_{12}(d) = (\mu/I_2)\int_{r=0}^{R1} r\, H_Z(r, d)\, dr \qquad \text{Eq. 18}$$

As another check on the accuracy of the Hz(r, d) spreadsheet calculations described above, I carried out this Eq. 18 integral numerically in an EXCEL spreadsheet and got excellent agreement with the textbook complete elliptic integral solutions for M_{12} of Eq. 19, integrating over $H_Z(r, d)$ results pasted in from the spreadsheet used to calculate the curves in Figures 4, 5 and 6.

Because Eq. 18 represents a double integral (because $H_Z(r, d)$ comes from the integral in Eq. 13) calculating mutual inductances from $B_Z(r, d)$ in a spreadsheet using Eqs. 13 and 18 is a bit of a chore. Fortunately much better mathematicians than I have been working on this problem for at least sixty or seventy years and have an analytical solution in terms of the complete elliptic integrals of the first kind, K(k) and the second kind, E(k). These have been available in table form for many years (such as in Jahnke and Emde, "Tables of Functions", since at least the 1938 edition [I use the 1945 edition], as well as Abromowitz and Stegun [but be careful as they

define the modulus, k, differently from J&E and most E&M texts]). Fortunately, they are also defined functions in engineering/scientific software packages such as the excellent "HiQ" package available for the Macintosh, and some other, computers. This makes it quite easy to generate the mutual (and self-) inductance data needed to analyze the practical inductor structures of interest. The analytic expression for M between two loops is

$$M = \mu\ [R_1 R_2]^{1/2} \{[(2/k) - k] K(k) - (2/k) E(k)\} \qquad \text{Eq. 19}$$

where the modulus of the complete elliptic integral functions, k, is given from

$$k^2 = (4 R_1 R_2)/[d^2 + (R_1 + R_2)^2] \qquad \text{Eq. 20}$$

Listing 1 shows a short (≈12 line) listing of HiQ "script" code that calculates $M(R_2)$ for any specified d and R_1 values and stores the results in an array for convenient graphing or pasting into EXCEL worksheets.

The functional dependencies are easier to understand if we rewrite Eqs. 19 and 20 in terms of normalized radii and heights, as in Eqs. 12 - 15. If we take one of the loop radii as fixed and call its radius, R, and call the other radius, r, and write the expressions in terms of the normalized dimensions, r/R and d/R, we have for Eq. 19,

$$M = \mu R\ (r/R)^{1/2} \{[(2/k) - k] K(k) - (2/k) E(k)\} \qquad \text{Eq. 21}$$

and

$$k^2 = 4\ (r/R)/[(d/R)^2 + (1 + (r/R))^2] \qquad \text{Eq. 22}$$

This form illustrates clearly how inductance is proportional to R, assuming all other geometric factors remaining in proportion. Values of M(r/R) for various heights, d/R, are shown in Figure 7. As is obvious in Figure 4 from the flatness of the B-field near the center of the loop for small values of d/R, and the fact that the integrated area in Eq. 18 varies as $(r/R)^2$ [or R_2^2 in Eq. 18], M must vary at least quadratically with r/R near r/R=0. As seen in Figure 7, this is indeed the case for d/R values under 0.5, and for d/R values near zero, the M(r/R) curves climb into a logarithmic singularity at r/R=1, as expected in light of the 1/(1-r/R) singularity in the B-field. Beyond r/R=1, the M(r) values drop off of the logarithmic singularity and decrease relatively slowly at larger r/R values. Very clearly, mutual inductance is maximized between equally sized loops spaced as closely together as possible. (That is, of course, just what a solenoidal inductor is!)

In the calculation of the inductance of the spiral inductor structure of Figure 1, we need to know the mutual inductances between coplanar (d=0) coaxial loops of different radii. While the M(r/R) curves in Figure 7 are drawn over the

$0 \le r/R \le 2$ range, for d/R=0 this is really not necessary. Since $M_{12} = M_{21}$, we can always reverse the definitions of the "fixed" radius, R, and the "variable" radius, r whenever r >R, as we do not have to worry about the d/R scaling. (Of course we will have to rescale the calculated mutual inductance by multiplying the value from a chart based on R=1 meter by the new, larger R value.) All of the M(r/R) information is contained within the $0 \le r/R \le 1$ range with the simple requirement for scaling with the magnitude of the larger radius, R. Figure 8 shows the curve of M(r/R) for d=0 in the $0 \le r/R \le 1$ range, along with a 10xM expanded curve. Numerical values from which these were plotted are found in the EXCEL 4.0 file "M(r/R) for Spiral Inductors v2C".

Figure 7 can also be used to find the self-inductances of loops for either spiral or solenoid inductor applications. Because of the 1/(R-r) B-field singularity for d=0, if the radius, a, of the conductor forming the loop were zero, then the self inductance of the loop would be infinite (although only logarithmically infinite). Hence, it is essential to specify the conductor radius, a, for calculation of loop self-inductance. As described in Van Duzer (section 5.24) or other texts, the external self-inductance of a loop is calculated by carrying out the surface integral in Eq. 17 to the interior edge of the conductor. I.e., we calculate the self-inductance for a circular loop of radius, R, by setting d=0 in Eq. 18 and carrying out the integral from r=0 to r=R-a (instead of r=0 to r=R as for mutual inductance). This also means we can, from Figure 8, pick off the external self inductance value, L_e, as the value for M corresponding to the normalized radius, r/R = (1 - a/R). (Of course, if the loop size is different from R=1 meter, then the M value must be multiplied by the actual value of R [in meters].) This may be expressed as,

$$L_e = M(r=R-a, d=0) \qquad \text{External Self-Inductance} \qquad \text{Eq. 23}$$

This external self-inductance value calculated in this way is not quite the entire self-inductance of the loop. As mentioned previously, at low frequencies (i.e., for $\delta >> a$, where δ is the skin depth in the conductor metal), the B-field drops linearly from the surface value to zero at the conductor center. This gives a very low-frequency internal inductance for a solid wire of $L_i = \mu/8\pi$ henrys/meter of wire length. Since the length of wire around a loop of radius R is $l = 2\pi R$, the very low frequency internal self inductance for a loop is

$$(L_i)_o = (\mu/4)\, R \qquad \text{Internal Self-Inductance (dc)} \qquad \text{Eq. 24}$$

at higher frequencies, the currents will flow closer to the surface of the inductor and the internal inductance will be smaller. Note that like the external self inductance (Eqs. 21 and 23), the internal self-inductance also scales with R. This internal self-inductance, Li, must be added to the external self inductance, Le, from Eq. 23 to get the total self-inductance of the loop,

$$L_s = L_e + L_i \qquad \text{Total Self-Inductance} \qquad \text{Eq. 25}$$

In the modeling of a solenoidal inductor as a stack of loops of equal radius, R, shown in Figure 2, we need not only this loop self-inductance value, L_o, but also the mutual inductances, M_{ij}, between loops separated by height, d, values integer multiples of the loop stacking pitch, S (or S/R in normalized form). Figure 9 shows a plot (data from file "R=r=1 Mutual Inductance vs d") of the mutual inductance, M, between equal radius (R=r=1 meter) coaxial loops vs. the normalized distance, d/R, separating them. An expanded 10xM curve is also included. Hence, Figure 9, together with Figure 8 for the loop self-inductance values, is all we need to calculate the inductance of multi-turn solenoids.

Calculation of the Inductance of Solenoids by Stacked Loop Method

Figure 2 shows the geometry considered for the modeling of a solenoid inductor by a series of stacked loops. As noted above, with the self- and mutual inductance data illustrated in Figures 8 and 9, all of the E&M part of the work in calculating the inductance for solenoids is done; what remains is a little circuit arithmetic. This is easier to see if we start from a simple case: two turns or two coupled loops. Since the same current flows through both loops, and the sense of current direction around the loops is the same (which means that the sign of the mutual inductance terms will be positive), the total voltage, V, induced by a rate of change of current, dI/dt, will be given by

$$V = L\, dI/dt = L_{1s}\, dI_1/dt + M_{12}\, dI_2/dt + L_{2s}\, dI_1/dt + M_{21}\, dI_1/dt \qquad \text{Eq. 26}$$

Since M12 = M21 (as seen from Eqs. 19 and 20, for example) and the fact that I2 = I1 =I, we must have that the total inductance for the two loops, L, is just

$$\begin{aligned} L &= L_{1s} + M_{12} + L_{2s} + M_{21} \\ &= 2\, L_s + 2\, M_{12} \qquad \text{for } L_{1s}=l_{2s}=L_s \text{ and } M_{21}=M_{12} \end{aligned} \qquad \text{Eq. 27}$$

Hence, the calculation of the solenoid inductance is simply a matter of summing up some loop self-inductances and mutual inductances between loops to get the answer. This is very simple. The only problem arises as the number of turns or loops, N. increases, the number of L and M terms to be looked up and added is N^2, which can get a bit tedious for large values of N.

Fortunately spreadsheets are ideal for doing this type of calculation where the arithmetic is simple but the organization of all of the data a bit troublesome. I created an EXCEL 4.0 spreadsheet (filename: "Any S/R Solenoid L Calc v3") to carry out this task. How this works is most easily seen by reproducing the example of Eq. 27 for a somewhat bigger case; we will consider five turns or loops. For N=5, we have

$$
\begin{aligned}
L = \; & L_{1s} + M_{12} + M_{13} + M_{14} + M_{15} \\
& M_{21} + L_{2s} + M_{23} + M_{24} + M_{25} \\
& M_{31} + M_{32} + L_{3s} + M_{34} + M_{35} \\
& M_{41} + M_{42} + M_{43} + L_{4s} + M_{45} \\
& M_{51} + M_{52} + M_{53} + M_{54} + L_{5s}
\end{aligned}
\qquad \text{Eq. 28}
$$

Notice that the upper left (2 x 2) corner of this square array is the same as the sum for the N=2 case in Eq. 27. Summing the upper left (3 x 3) corner gives the inductance for an N=3 loop solenoid, etc., just as long as we order the loops sequentially (i.e., it is assumed that we mean 3 "adjacent" loops in a stack when we refer to a 3-turn solenoid). Eq. 28 illustrates that one mutual inductance array can be used to calculate the inductance of a solenoid with the specified dimensions (radius, R, loop and turns pitch, S, [entered as S/R]) for any number of turns, N, from N=1 to N=[dimension of array] (N=5 for Eq. 28). In the "Any S/R Solenoid L Calc v3" spreadsheet, the M array size is 21 x 21, so the inductance of up to N=21-turn solenoids can be calculated. (It is trivial to extend the size of the arrays, if desired, to accommodate larger numbers of turns.)

The way the spreadsheet works is to first set up another square array that calculates, from the relative positions of any two loops in the stack, the distance between them, d/R. This separation distance, d/R array is used as the index to a mutual inductance lookup table (the large data file "R=r=1 Mutual Inductance vs d" is included in the "Any S/R Solenoid L Calc v3" spreadsheet to look up the M(d/R) values, since EXCEL doesn't, to my awareness, have the complete elliptic integral functions [K(k) and E(k) in Eqs. 19 and 21] available in it to calculate M(r/R). There is also an issue of calculation of the self-inductance of the loops. Rather than include the entire "M(r/R) for Spiral Inductors v2C" file in this spreadsheet as a lookup table, you have the option of either pasting in an exact L_e value from this file for the specified conductor radius, a/R, (Eq. 23), or you can omit the number or put in zero for this "Lext" value, and the approximate L_e value,

$$L_e \approx \mu R \, [\ln(8/(a/R)) - 2] \qquad \text{for } a/R \ll 1 \qquad \text{Eq. 29}$$

will be used (Van Duzer, Section 5.24). The "bottom line" for this "Any S/R Solenoid L Calc v3" spreadsheet is a table of inductance, L, vs. number of turns, N, values for integer values of N from N=1 to N=21 (as the arrays are sized now).

For the case of the solenoid inductor, there are a number of reasonably good equations which give at least pretty good approximations to the inductance to an air-core solenoid over a fair range of design parameters. The simplest, fairly accurate, formula (appearing in F. E. Terman, "Radio Engineering Handbook" for 1943 and most other handbooks and texts) is

$$L = (\pi \mu N^2 R)/[0.9 + 1/R] = (\pi \mu N^2 R)/[0.9 + N (S/R)] \qquad \text{Eq. 30}$$

where in the second version, the nominal length of the inductor, l, has been replaced by $l = N S$, where S is the turns pitch as shown in Figure 2. A much more sophisticated formula is given in Jahnke and Emde (p. 87, with tables on pp. 88-89)

$$L = (2/3)\,\mu\, R\, N^2 \{ [K(k) + ((d/l)^2 - 1)E(k)]/\sin\alpha - (d/l)^2 \} \qquad \text{Eq. 31}$$

where $d = 2R$ is the diameter, l the length, and α is defined by $\tan\alpha = d/l$. The fact that this formula for the inductance of thin-walled solenoids is based on the K(k) and E(k) complete elliptic integral functions (like Eqs. 19-22) gives on a certain degree of confidence in its rigorousness. Listing 2 shows a short listing of HiQ "script" code that calculates L vs. N from Eq. 31, again taking $l = N S$ for the length. Both Eqs. 30 and 31 were used for comparison with the "Any S/R Solenoid L Calc v3" spreadsheet calculation. As seen in Figures 10-13, in general the results were quite close, particularly between my "stacked loop" spreadsheet calculation and the J&E formula (Eq. 31). For S/R=0.2 in Fig. 10, the inductance numbers from both the "Terman Formula" (Eq. 30) and the "Jahnke and Emde" formula (Eq. 31) are nearly identical with the results from this "Stacked Loop Calc" spreadsheet calculation. As seen for S/R=0.025 (an extremely fine pitch; S/R=0.2 with R≈0.0006 meters is thought to be about the limit for simple wirebond embedded inductors in MCM's) in Figure 12b, the percentage differences tend to be larger for fewer numbers of turns, and the agreement is better with the J&E formula (Eq. 31). This is clear on a log plot like Figure 12b, but not on the linear plots like Figure 12a. Note that for a fairly wide turns spacing, S/R=0.4 in Figure 13, this "Stacked Loop Calc" spreadsheet calculation gives about a 10% higher L (for a/R=0.03) than Eqs. 30 or 31. Since with larger spacings the self-inductance assumes higher importance (because the mutual inductances are relatively smaller), my guess would be that the stacked loop calculation is probably closer to reality.

The results for solenoid inductance calculations using this "Any S/R Solenoid L Calc v3" spreadsheet, L vs. N for integer values of N from 1 to 21, for nine different S/R values are plotted on Figures 14 (linear scale) and 15 (log scale), with numerical data presented in Table 1. It should be pointed out that there is much more data available in the calculation than is presented in this summary. In particular, the mutual inductance array is available (e.g., Eq. 28), such that the details of the coupling are known on a turn-by-turn basis. This would be invaluable, for example, if the turns were split off into two or more different circuits; the M array would provide precise information for the transformer design and characterization.

Calculation of L for Planar Spiral Inductors by Stacked Loop Method

Figure 1 shows the geometry considered for the modeling of a planar spiral inductor by a series of nested loops. Because all of the loops lie in the same plane, all of the E&M part of the work in calculating the inductance that we need is summarized in Figure 8 alone. Basically, the circuit arithmetic is the same as

described above (Eqs. 26-28) for the solenoid case, except that since the loop radii are all different, the Ls values will all be different and we have to remember to scale the inductance values looked up out of an R=1 meter table by multiplying them by the actual R [in meters]. The scaling for the planar spiral inductor is based on the radius of the center of the conductor of the outermost (N=1) loop. The loops (turns) are numbered consecutively from the outside inward. While the spreadsheet calculation (flienname: "Spiral Inductor L(N,S/R) CalcV1") is capable of supporting irregular turns pitches, in the calculation the turns pitch, S, is taken as constant (entered in normalized form as S/R). Hence, the N=1 loop has radius R, the N=2 turn has r=R-S, N=3 has r=R-2S, etc. In general the radius of the Nth turn of the spiral is

$$r(N) = R\,[\,1 - (N - 1)(S/R)\,] \qquad \text{Eq. 32}$$

Obviously, since r(N) cannot be negative, for any given value of S/R, there is only room for a certain number of turns in the spiral. It turns out that keeping track of that fact is the biggest factor in making the "Spiral Inductor L(N,S/R) CalcV1" spreadsheet calculation a lot more complicated than for the solenoid case. However, the approach is identical, the goal being to build up the inductance array like Eq. 28. The "M(r/R) for Spiral Inductors v2" data used to plot Figure 8 is included in the spreadsheet as a lookup table for the loop-to-loop mutual inductance values (and for the loop self-inductance values as well, using r=R-a [Eq. 23]).

The results, including both the L(N) data and the inductance array (M array), from this "Spiral Inductor L(N,S/R) CalcV1" spreadsheet calculation for S/R values of 0.5, 0.4, 0.35, 0.3, 0.25, 0.2, 0.175, 0.15, 0.125, 0.11, 0.10, 0.09, 0.08, 0.07, 0.06, 0.05, 0.04, 0.03, 0.02 and S/R=0.01 , all with conductor radius a=0.4(S/R), are summarized in the file "R=1m Spiral Inductor L(N,S/R).S". This is important because it contains the mutual inductance array (e.g., Eq. 28) for each case, such that the details of the coupling are known on a turn-by-turn basis. This would be invaluable, for example, if the turns were split off into two or more different circuits; the M array would provide precise information for the spiral transformer design and characterization.

The problems with planar spiral inductors are fairly apparent from the curves in Figure 16. Unless the S/R value is extremely small (and such small S/R values lead to very small conductor dimensions, high resistance and generally degraded Q values), the difference in radius between the loops leads to poor coupling (low mutual inductance) between turns. This, and the smaller sizes of the loops as their radii decrease as N increases, leads to the rapid saturation of the increase of L with N in spirals. This is more apparent in the log-log plot in Figure 17 (where the slope is the power of N with which L(N) is increasing). Contrast the curves for practical values of S/R (e.g., S/R≤0.2 for low resistance) for the spirals in Figure 17 with the equivalent log-log plot for the solenoid inductors with various S/R values in Figure 18. The planar spiral is convenient for fabrication as an embedded MCM inductor. Unfortunately that is about all the good that can be said of it, since it is electrically substantially inferior to the solenoid inductor structure.

Dependence of Bandwidth, Q and Noise on R_{ac} of Inductor

The prime specification for an embedded MCM inductor, next to that of its inductance, L, is its Q at a given frequency, f, which is defined as π times the maximum energy stored divided by the energy dissipated per half cycle.

$$Q(f) = \pi \text{ (maximum energy stored)/(energy dissipated per cycle)} \qquad \text{Eq. 33}$$

With a sinewave current,

$$i(t) = i_p \sin(2\pi f t) \qquad \text{Eq. 34}$$

through an inductor having an inductance, L, and an ac series resistance, R_{ac},

$$\text{maximum energy stored} = (1/2)\, L\, i_p^2 \qquad \text{Eq. 35}$$

and the average power dissipation in the series resistance, Rac, is

$$\text{average power dissipation} = R_{ac}\, I_{rms}^2 = R_{ac}\, (i_p/\sqrt{2})^2 = (1/2)\, R_{ac}\, i_p^2 \qquad \text{Eq. 36}$$

so that the energy dissipated per half cycle (i.e., in a period of time t=1/2f), is just

$$\text{energy dissipated per half cycle} = \text{average power dissipation}/(2f) = [(1/2)\, R_{ac}\, i_p^2]/(2f) \qquad \text{Eq. 37}$$

so that from Eqs. 33, 35 and 37, the inductor Q at the signal frequency, f, is given as

$$Q(f) = \pi\, [(1/2)\, L\, i_p^2]/\{[(1/2)\, R_{ac}\, i_p^2]/(2f) = 2\pi f\, L/R_{ac} \qquad \text{Eq. 38}$$

Since the angular frequency (radians per second) is just $\omega = 2\pi f$, this is frequently written equivalently as

$$Q = 2\pi f\, L/R_{ac} = \omega\, L/R_{ac} \qquad \text{Eq. 39}$$

The factor of π in the definition of the Q of an inductor (Eq. 33) comes from the original definition of Q in terms of the bandwidth of a simple resonant circuit. If the inductor, L, is connected in parallel with a capacitance, C, for $R_{ac}=0$ (or $Q=\infty$), the circuit will resonate at a frequency $\omega_o = 2\pi f_o$ given by

$$\omega_o = 2\pi f_o = 1/\sqrt{(LC)} \qquad \text{Eq. 40}$$

For finite loss (finite Q), $R_{ac} \neq 0$, the series RLC circuit resonates at a frequency, ω_r

$$\omega_r = 2\pi f_r = \omega_o [1 - (1/2Q)^2]^{0.5} \qquad \text{Eq. 41}$$

where the finite Q resonant frequency, ω_r, is very slightly lower than the lossless ($Q=\infty$) resonant frequency, ω_o (e.g., 0.0078% lower for Q=40 or 0.125% lower for Q=10). If this RLC resonant circuit is driven by an ac current source, the voltage will reach a peak value at the frequency f_r, and drop to a voltage of $1/\sqrt{2}=0.7071$ times this peak value at frequencies Δf above and below this (the half-power points), where, for reasonably high values of Q, Δf is given by

$$\Delta f = f_r/(2Q) \qquad \text{Eq. 42}$$

Using the usual definition of bandwidth as the frequency difference between the half-power points (or about -3dB voltage points), or BW=2ΔF in this case, we have,

$$Q = f_r/2\Delta f = (\text{resonance frequency})/(\text{bandwidth})_{3db} \qquad \text{Eq. 43}$$

which was the original definition of Q used in rf circuit work. Hence, the factor of π in the energy definition of Q (Eq. 33) is required for compatibility with the earlier rf circuits definition (Eq. 43).

In this "reasonably low loss" (e.g., Q above 5 or 10) case, the parallel resonant circuit (capacitor C in parallel with inductor L, with its series resistance, R_{ac}) at resonance looks essentially like a pure resistance, R_p, whose value is given by

$$R_p \approx Q^2 R_{ac} \qquad \text{at } f = f_r \qquad \text{Eq. 44}$$

If Eq. 44 at first glance males it appear that increasing Rac would increase Rp, this is wrong, as increasing R_{ac} <u>decreases</u> Q (Eq. 39), so, due to the Q^2 term in Eq. 44, R_p <u>decreases</u> with increasing R_{ac}. This may be clearer when the expression for Rp at resonance is written differently,

$$R_p \approx 1/[(\omega C)^2 R_{ac}] = |Z_c|^2/R_{ac} \qquad \text{at } \omega=\omega_r \qquad \text{Eq. 45}$$

where $|Z_c|=1/\omega C$ is the magnitude of the capacitor impedance at $\omega=\omega_r$, or equivalently as

$$R_p \approx (\omega L)^2/R_{ac} = |Z_l|^2/R_{ac} \qquad \text{at } \omega=\omega_r \qquad \text{Eq. 46}$$

where $|Z_c| = \omega L$ is the magnitude of the inductor impedance at $\omega=\omega_r$. Both of these forms show that R_p indeed is proportional to the inverse of Rac, so that for highest impedance in the resonant circuit, the ac resistance, Rac must be kept as small as possible. Also, it can be shown that the equivalent thermal noise current (Johnson noise) for the resonant circuit is the same as that calculated for a resistor of value R_p.

Magnetic Field Intensity/Current Distribution on Solenoid Conductor

As seen in the previous section, the performance quality of an inductor, in terms of attainable impedance, bandwidth, Q, noise, efficiency, etc. is critically related to just how low the effective series resistance of the inductor, R_{ac}, can be made. As discussed in my report of 6/1/96, external factors such as dielectric losses in substrate materials can lower the Q values of MCM embedded inductors if substrates like silicon are used, normally the limiting factor for R_{ac} is the skin effect losses in the conductors. (For ferrite or other ferromagnetic core inductors with substantial relative permeabilities [$\mu_r >> 1$], the core material losses can dominate, but we will be considering principally the case of non-magnetic [air or other $\mu_r=1$] core inductors here.)

Calculation of the dc resistance, R_{dc}, of a metal conductor having resistivity, ρ, is quite simple, since for most geometries the resistance per unit length, R_{dc}/l, is given from the cross-sectional area, A_c, as

$$R_{dc}/l = \rho/A_c \qquad \text{Eq. 47}$$

(The exception is geometries for which the direction of current flow or cross-sectional area of the conductor changes very rapidly along the current path, such as at sharp corners in conductors or abrupt changes in conductor size, but these are not serious issues in most inductor geometries.) For example, the dc resistance of a circular wire of radius a or diameter $d_W=2a$ will be given by

$$R_{dc}/l = \rho/(\pi a^2) = 4\rho/(\pi d_W^2) \qquad \text{for Circular Wire} \qquad \text{Eq. 48}$$

Unfortunately, things are not so simple for the case of the ac skin-effect resistance of conductors in inductors. There are in fact expressions for the ac skin-effect resistance, R_{ac}, of certain specific conductor geometries, such as that of a circular wire used as the center conductor of a coaxial cable, but if the same wire is wrapped with very close turns spacing around a core to make a solenoid inductor, this coax line expression for R_{ac} will not give the correct value of the ac resistance of the wire. The problem is that of "current crowding", or non-uniform distribution of ac current around the conductor periphery. Because of the circular symmetry of a coaxial line, the current flows uniformly around the periphery of the center conductor wire, even as the skin effect forces the current to flow nearer and nearer to the surface as frequency is increased. This uniformity of the skin-effect current around the center conductor of a coaxial line is a direct reflection of the uniformity of the tangential magnetic field around the surface of the conductor. (This is just a specific instance of the general magnetics principal that the change in tangential magnetic field, H_t (in amperes per meter) at the surface of a conductor equals the surface current density, J_s, flowing in the conductor.

In the case of a solenoid, the magnetic field at the surface of the conductors is strongly influenced by the overall form of the inductor, not just by the local shape of the conductors as in a coaxial line. This could have important implications. For example, in the idealized view of a solenoid inductor, the magnetic field is strong inside the solenoid, and essentially zero outside. If that is the case, then the high-frequency surface current on the conductors (since the surface current density must equal the tangential H-field at the surface) would be near zero on the outside of the conductor, and hence the conductor loss would be essentially twice as large as you might otherwise think, since with this "current crowding", only half of the periphery contributes to conduction. Also, this would mean that the substrate metal return path in a wirebond inductor might as well be made only half as many skin depths thick as would ordinarily be specified, since the bottom side wouldn't contribute to high-frequency conduction anyway. (As I will show later, this turns out <u>not</u> to be the case for geometries of interest.) In any event, in order to calculate R_{ac} for the conductors in a solenoid, or other inductor structures, we must first examine the magnetic field distribution around the conductors, in order to determine what expression for R_{ac} should be suitable for use in that geometry.

The geometry for the calculation of the solenoid magnetic field was shown previously in Figure 2, and the stacked-loop calculational approach in which the magnetic field at any point in the solenoid is obtained as the sum of the fields from each individual loop at that point (Figures 3-6). Note that in these H(r/R) plots, what is plotted is the z-component of magnetic field, $H_Z(r/R)$, versus radial distance from the axis of the solenoid, measured in the plane of symmetry normal to the axis passing through the center of the center loop of the solenoid. This is convenient in that in this plane of symmetry, $H(r/R)=H_Z(r/R)$ since $H_r=0$ by symmetry. This means, of course, that only odd numbers of loops (turns) in the solenoid can be treated, but this plane gives the worst-case field differences between the inside and outside of the conductors. Figure 19a shows $H_Z(r/R)$ for a turns pitch, S, to loop radius, R, ratio of S/R=0.2 (a comfortable value even for modest-sized wirebond loops) for r/R=0 (axis of solenoid) to r/R=2 (outside of the solenoid loops by one loop radius) for solenoids of N=1, 3, 5, 7, 9, 11 and 13 turns. Note that initially the field on the axis, $H_Z(r=0)$, is nearly proportional to the number of turns, indicating reasonably strong coupling between 1st and 2nd nearest neighbor loops, but the increase in $H_Z(r=0)$ is small between, for example, N=11 and 13 turns because of the substantial axial distance to these end turns (1.2R). On the other hand, as the total length of the solenoid becomes large (e.g., 2.4R for N=13 turns with S/R=0.2), the field distribution within the solenoid (r/R<1) becomes much flatter, and much larger than the field outside. For example, for N=13 turns, H_Z=3.97 ampere-turns/meter (A/m) at r=0, increasing to 4.21 A/m at r=0.8R, while outside the solenoid at r=1.2R the field is only H_Z=-0.6 A/m.

While the gross solenoid field in Figure 19a, particularly for larger numbers of turns, is much higher inside the loops than it is outside, to understand the implications of the field distribution on the ac skin-effect resistance of the

conductors, we must look in detail at the fields immediately adjacent to the surface of the wires. The field in this region (near r=R) is shown in detail in Figure 19b. Remember that the stacked-loop calculation of $H_Z(r)$ for the solenoids in Figures 19-25 assume an extremely small conductor radius for the loops, which leads to the near-singularity in $H_Z(r)$ at r=R. This is just fine, since it is understood that for a given actual conductor radius, a, the external $H_Z(r)$ field shown in the Figures is correct for the region outside the conductor (i.e., for $r \leq (R-a)$ and $r \geq (R+a)$). At dc, the H_Z-field within the metal conductors drops linearly from the value at the surface (r=(R-a) or r=(R+a)) to zero at the center (r=R) (this is for a straight circular wire; it will be slightly off-center for a solenoid). For higher frequencies, the dropoff of the H-field as one goes away from the surface is more rapid, determined by the skin depth, δ. It is the details of this dropoff in H-field within the conductor (since it mirrors the surface current density within the conductor) that determines how the ac resistance is to be calculated. Note that because of the 1/(R-r) dependence of the H-field near the conductor, the vertical scale factor has been compressed from ±8 A/m in Figure 19a to ±20 A/m in Figure 19b. At this scale factor, it is clear in Figure 19b that at small distances from the center of the loop conductor (r/R near 1), the dominant effect is that of the 1/(R-r) behavior of the H-field around circular wires, as opposed to the solenoid shape effects. For example, even for a fairly large diameter conductor, a/R=0.03, the surface H-field (and correspondingly, the surface current on the conductor, J_S) at its highest point (r=R-a or r/R=0.97 in Figure 19b) varies from 5.76 to 7.57 A/m for N=1 to 13 turns, while the field at the lowest point on the outside surface varies from -4.87 to -3.78 A/m, so that the variation (Eq. 52) is from ±8.4% at N=1 to ±33% at N=13, with a variation of ±21% for N=5, a more typical number of turns. Since these numbers represent the extremes in surface current density over the conductor wire surfaces, simply using the same expressions for R_{ac}, the ac skin effect resistance, as for a straight wire (such as the center conductor of a coaxial line) should be quite accurate.

For larger values of the solenoid turns pitch, S, such as the S/R=0.4 case shown in Figure 20a and 20b, this trend is even clearer. The gross $H_Z(r)$ field within the solenoid is quite uniform (Figure 20a for r/R<0.8) for larger numbers of turns because of the greater length of the solenoid (4.8R for N=13 turns), but the field strength at the center is lower than in Figure 19a because of the reduced coupling between the more widely spaced turns. This also means that the fields at the surface of the conductors is even more uniform for S/R=0.4 in Figure 20b than for S/R=0.2 in Figure 19b, ±23% at N=13 or ±17.5% at N=5 (at N=1 it is the same as in Figure 19b, of course). Hence the use of a straight-wire formula for R_{ac} is even better justified for this S/R=0.4 case.

In the opposite direction, to solenoids with tighter (finer) wiring pitches, nCHIP has fabricated wirebond solenoids (details of which will be discussed later) which have loop areas equivalent to that of an R=0.00107 meter radius circle with a turns pitch of S=98.2 μm using 1 mil diameter wire, and it appears reasonable to achieve a pitch of S=125 μm with 1.5 mil diameter wire (radius, a=19.05 μm), which

corresponds to S/R=0.1169 and a/R=0.0178. Hence, the S/R=0.1 case illustrated in Figures 21a and 21b is probably representative of the practical limit for fine pitch in MCM wirebond solenoids. (nCHIP's 1 mil wire example has S/R=0.0918, but the Q is poorer because of the smaller wire size, and the difference in surface fields, which depends principally on a/S is worse for the 1.5 mil wire on 125 μm pitch case than for the 1.0 mil wire on 98.2 μm pitch.) We note in Figure 21a the tight coupling between turns as evidenced by the nearly linear increase of $H_Z(r=0)$ with N up to 7 to 9 turns (curves for N=1, 3, 5, 7, 9, 11, 13, 15, 17, 19 and 21 turns are shown in Figures 21a and 21b). As would be expected, the inside/outside field variation is larger for this fine turns pitch case. However for a wirebond conductor radius of a/R=0.0178, at N=5 turns the field uniformity is ±15%, and even for N=21 turns, it is ±34%.

Inasmuch as a ±34% variation in surface current density over the periphery of the conductor wire is significant, it is worth calculating how much such a non uniformity in current density would be expected to perturb the accuracy of a calculation of the wire high-frequency resistance, R_{ac}. If we make the assumption that the surface current density around the conductor is sinusoidal, that is,

$$J_S(\phi) = J_a + J_p \sin(\phi) \qquad \text{Eq. 49}$$

where J_a is the average value of surface current around the wire and J_p/J_a represents the field uniformity figure as quoted above, while ϕ denotes the angular position around the wire (with $\phi=0$ directed parallel to the solenoid axis, $\phi=\pi/2$ the peak field point on the inside of the loop and $\phi=3\pi/2$ the minimum field point on the outside if the loop). The use of a straight-wire value for R_{ac} would be assuming that the value of J_S was everywhere the same as its average value, Ja. Because power dissipation varies as J_S^2, the non uniform current distribution in Eq. 49 will give a higher power dissipation, and hence a higher value for R_{ac}, than the uniform straight-wire case. The difference between the actual solenoid R_{ac} value, $(R_{ac})_{sol}$, and the straight-wire calculated R_{ac} value, $(R_{ac})_{coax}$, will be given by

$$(R_{ac})_{sol}/(R_{ac})_{coax} = [\text{Average}(J_S(\phi)^2)]/[\text{Average}(J_S(\phi))]^2$$

$$= [(1/2\pi)\int_0^{2\pi} [J_S(\phi)]^2\, d\phi\,]/[\,J_a\,]^2 \qquad \text{Eq. 50}$$

which, substituting Eq. 49 for $J_S(\phi)$ and carrying out the integral gives

$$(R_{ac})_{sol}/(R_{ac})_{coax} = [\,J_a^2 + 0.5\,J_p^2]/(J_a^2)$$

$$= 1 + 0.5\,(J_p/J_a)^2 \qquad \text{Circular Conductor} \qquad \text{Eq. 51}$$

where J_p/J_a is the same as the field uniformity values cited above. Specifically, for a wire radius, a, and solenoid loop radius, R, the value of J_p/J_a is given by

$$J_p/J_a = [H_z(R-a) - H_z(r+a)]/[[H_z(R-a) + H_z(r+a)] \qquad \text{Eq. 52}$$

(where magnitudes, rather than signed quantities, have been assumed for the $H_z(R-a)$ and $H_z(r+a)$ values). For the S/R=0.1, a/R=0.0178 wirebond solenoid example cited above (Figure 21b), for N=5 we found J_p/J_a = 15%, which, from Eq. 51 gives $(R_{ac})_{sol}/(R_{ac})_{coax}$ = 1.0115 (which means only a 1.15% error assuming a straight-wire loss expression), or for the extreme N=22 turns case, for which we found J_p/J_a = 33.7%, Eq. 51 gives $(R_{ac})_{sol}/(R_{ac})_{coax}$ = 1.0567, or a 5.67% error in using a straight-wire calculation of R_{ac} for a solenoid. This is a very reasonable error for an inductor Q calculation, and the correction factor from Eq. 51 can always be used to correct the solenoid R_{ac} values calculated using a straight circular conductor expression for R_{ac}.

Figures 22a and 22b (for S/R=0.05) and 23a and 23b (for S/R=0.03) are illustrative of what more conventional (tightly wound, S≈2a, insulated wire single-layer) solenoids look like. Inasmuch as there appears no practical way to fabricate such fine pitches in a wirebond solenoid for an MCM, these are included here for reference only. The S/R=0.03 case of Figures 23a and 23b does, however serve as an excellent starting point to examine another important problem; the use of stripe or ribbon elements in fabricating mixed-signal MCM embedded inductors. One example of this would be the use of ribbon bonds in place of ordinary round wire wirebond loop conductors. Another is the need to analyze the R_{ac} for metal microstrip return paths for wirebond inductors (in which the wirebonds form the top half of the solenoid loops while substrate metallization stripes form the bottom return path. We would like to have some insight into the fields associated with these flat conductor structures similar to what is shown in Figures 19-23 for circular conductors in solenoids. Such an example was carried out using the stacked-loop approach. The geometry for this calculation is shown in Figure 24. Here, a ribbon conductor of dimensions 0.03R x 0.15R is simulated with a stack of 5 circular cross-section conductors, each carrying a current of 0.2 A (to give 1 A total conductor current, as in the previous examples). These ribbon conductors (e.g., 7 loops as shown in Figure 24) are stacked on a pitch of S/R=0.21 to complete the solenoid. Figures 25a and 25b show the $H_z(r/R)$ plots for N=1 to N=7 turns (ribbon conductor loops) of the 0.03R x 0.15R conductors. Note that the gross fields for the ribbon solenoid in Figure 25a look virtually the same as for the S/R=0.2 circular conductor case in Figure 19a. The more detailed field plots near the conductors show much lower fields near the ribbon conductor surface in Figure 25b than for the circular conductor in Figure 19b. This is expected, of course, because of the width of the ribbon, which avoids the strong 1/(R-r) dependence of Hz(r) near the conductor). For example, at the inner surface of the ribbon conductor, r=0.985 in Figure 25a, for N=1 turn, $H_z(0.985)$=3.596 A/m, as compared to $H_z(0.985)$=11.11 A/m for the round

conductor in Fig. 19b (3.1x higher), while for N=7 turns, $H_z(0.985)$=4.72 A/m for the ribbon solenoid vs. $H_z(0.985)$=14.36 A/m for the circular wire. The field at the outside solenoid surface is $H_z(r/R=1.055)$=-2.85 A/m for N=1 turn and -2.06 A/m for N=7 turns for the ribbon solenoid (as compared to -10.1 A/m for N=1 and -9.3 A/m for N=7 with circular wire). This gives a current uniformity from Eq. 52 for the ribbon solenoid of J_p/J_a=±11.6% for N=1, increasing to J_p/J_a=±39.2% for N=7. (The circular wire was more uniform at 4.71% at N=1 and 21.4% for N=7 turns.)

If the field distribution around the periphery of the ribbon conductor varied sinusoidally as assumed for the circular conductors in Eqs. 49-51, then the correction factor for the ac resistance would be $(R_{ac})_{sol}/(R_{ac})_{coax}$ = 1.0067 for N=1 for the ribbon loop and $(R_{ac})_{sol}/(R_{ac})_{coax}$ = 1.0769 for the N=7 turn solenoid. If the surface current distribution were flat (constant high value, $J_s=J_a+J_p$, on the inside and a constant lower value, $J_s=J_a-J_p$, in the outside), then the integral averaging process would give, in place of Eq. 51,

$$(R_{ac})_{sol}/(R_{ac})_{plate} = [J_a^2 + J_p^2]/(J_a^2)$$

$$= 1 + (J_p/J_a)^2 \qquad \text{Flat Conductor} \qquad \text{Eq. 53}$$

Using this uniform field (worst case) correction factor, we would have the correction factor for the ac resistance as $(R_{ac})_{sol}/(R_{ac})_{coax}$ = 1.0134 for N=1 for the ribbon loop and $(R_{ac})_{sol}/(R_{ac})_{coax}$ = 1.154 for the N=7 turn ribbon solenoid. This is still a reasonably small correction factor, but it should not be omitted from wirebond solenoid Q calculations.

Skin-Effect Surface Impedance of Thick Metal Conductors

The dominant effect determining the high-frequency losses or Q in inductors is the "skin effect", or reduction of the depth of penetration of ac fields into conductors as frequency increases. The depth of penetration, or skin depth, δ, is given in any E&M text (e.g., Ramo, Whinnery and Van Duzer, "Fields and Waves in Communications Electronics", sections 4.12 and 5.14) for a frequency, f, as

$$\delta = [\rho/(\pi\mu f)]^{0.5} \qquad \text{Eq. 54}$$

where for most metals of interest as conductors (non-ferromagnetic, μ_r=1, metals) the magnetic permeability, $\mu=\mu_o\,\mu_r$, is just $\mu=\mu_o=4\pi$ x 10-7 henries/meter. The values for 20°C metal resistivity, ρ, in Eq. 54 are taken here as ρ=1.7241x10-8 Ω-m for copper, ρ=2.440x10-8 Ω-m for gold and ρ=2.620x10-8 Ω-m for aluminum. The skin depth, δ, as given by Eq. 54, is defined by the exponential attenuation of the electric field strength of a normal-incidence plane wave onto a flat plate of the conductor, of

thickness large in comparison to δ, where the magnitude of the field strength at a depth x into the conductor decays as $e^{-x/\delta}$. This leads to a surface impedance (internal impedance for a unit length and width of the conductor), Z_S, for the angular frequency $\omega=2\pi f$, given as

$$Z_S = R_S + j\omega L_i \qquad \text{Eq. 55}$$

where the real part (the surface resistance, R_S, from which R_{ac} is obtained) is

$$R_S = \rho/\delta = [\pi f \mu \rho]^{0.5} \qquad \text{Eq. 56}$$

and the imaginary part (internal inductance in surface region of the conductor) is

$$L_i = \rho/(\omega\delta) = R_S/\omega \qquad \text{Eq. 57}$$

Figures 26, 27 and 28 show convenient plots of the skin depth, δ, and surface resistance, R_S versus frequency for copper, gold and aluminum metal conductors respectively.

As an example of the use of Rs to calculate the ac resistance of a conductor, consider the case of a thick (metal thickness, $t_m >> 2\delta$) straight metal plate conductor of width, w (an example might be a stripline signal conductor. While the dc resistance of this plate, from Eq. 47 is given as

$$R_{dc}/l = \rho/A_c = \rho/(t_m\, w) \qquad \text{Eq. 58}$$

the ac resistance, R_{ac}, is obtained, assuming uniform field around the periphery, from the surface resistance, R_S, and the periphery, 2w (assuming here that $t_m << w$, so that the actual periphery [$=2w+2t_m$] is approximately equal to 2w), is given by

$$R_{ac}/l = R_S/[\text{periphery}] = R_S/(2w) \qquad \text{Eq. 59}$$

In addition to the requirements for the validity of Eq. 59 that the conductor be much thicker than 2δ and that the magnetic field be reasonably uniform around the periphery of the conductor, there is an additional requirement that the radius of curvature of the surface of the conductor be much larger than the skin depth, δ. For example, for a circular wire with radius, a, much greater than δ, Rac is given by

$$R_{ac}/l = R_S/(2\pi a) \qquad \text{Circular Wire for } a >> \delta \qquad \text{Eq. 60}$$

When $a << \delta$, Eq. 48 can be used. In between, things are <u>much</u> more complicated.

Calculation of the ac Resistance, R_{ac}, for Circular Cross-Section Wire

The low-frequency ($a << \delta$, Eq. 48) and high-frequency ($a >> \delta$, Eq. 60) expressions for the resistance of circular cross-section wires are very simple, but in between these asymptotic regions the expressions for Rac are rather messy (see Ramo, Whinnery and Van Duzer sections 5.16, 5.17 and 5.18). Defining $q = (a\sqrt{2})/\delta$, we have for R_{ac}/l (in ohms/meter) for a circular wire of radius a,

$$R_{ac}/l = [R_s/(\pi a\sqrt{2})][Ber(q)\, Bei'(q) - Bei(q)Ber'(q)]/[(Ber'(q))^2 + (Bei'(q))^2] \quad \text{Eq. 61}$$

while the internal inductance of the circular wire is given by

$$\omega L_i/l = [R_s/(\pi a\sqrt{2})][Ber(q)\, Ber'(q) - Bei(q)Bei'(q)]/[(Ber'(q))^2 + (Bei'(q))^2] \quad \text{Eq. 62}$$

In these expressions, Ber(q) and Bei(q) refer to the real and imaginary parts of the Jo Bessel function of a complex argument (referred to as Kelvin functions) which fortunately are available in tables and are defined functions in advanced math packages such as "HiQ" (and presumably Mathematica). Ber'(q) and Bei'(q) refer to the first derivatives of these functions, which are not tabulated or defined functions in math packages, but which may be obtained by performing numerical differentiation operations on the Ber and Bei functions.

The "HiQ" script used to calculate the ac resistance per meter, Rac/l, and the internal inductance, Li/l (referred to as Lint or Lint/l in the calculations and plots) is shown in Figure 29. This code was originally developed as part of a calculation of the transient response of small (hence lossy) coaxial lines, in which the transient response is obtained by taking an 8192-point IFFT (inverse Fourier transform) of the complex frequency-domain response. Because of the substantial number of frequency points involved, the code was streamlined to approximate the expressions in Eqs. 61 and 62 where possible (at higher frequencies) with analytical approximations I developed. These are far more accurate than Eq. 60 (which gives 6% to 7% errors for 1.5 mil bond wires even at f=1GHz), and can avoid the need for getting involved in the messy Ber/Bei calculations in some frequency ranges.

Figures 30a and 30b show the results of calculations of R_{ac}/l (in Ω/m) and L_i/l (plotted in nH/m so that it can be plotted on the same scale as R_s) for 1.5 mil (0.0015" diameter, or a=0.00001905 meter radius) straight circular wires made of aluminum, gold and copper. Figures 31a and 31b show the same for 1.0 mil diameter (a=0.00001270 meter radius) wires. As expected from Eq. 48, a comparison of Figures 31a and 31b with 30a and 30b shows that the calculated R_{dc}/l is 2.25x larger for the 1.0 mil diameter wires as compared to 1.5 mil wires of the same material, while at 200 MHz, R_{ac}/l for 1.0 mil wires is about 1.58x larger than for 1.5 mil, or at 1 GHz, about x1.54 larger (as compares to the factor of 1.50 suggested from Eq. 60, with the absolute values of R_{ac} from Eq. 60 in error by a substantial factor).

Calculation of the Q of a Circular Solenoid (Circular Wire Coil)

Since we have the capability for calculating both the inductance, L, (through the stacked-loop approach, as used for Figures 10 - 15 and 18 and Table 1, as executed in the EXCEL spreadsheet calculation, "Any S/R Solenoid L Calc v3") and the ac resistance, R_{ac}, of the conductors (Figures 29-31), we can calculate the Q of a wire solenoid inductor from Eq. 39. EXCEL spreadsheet calculations (filenames: "1.5 mil Al Solenoid L, Q(f) V2" and "1.0 mil Al Solenoid L, Q(f) V1" [the latest versions of the calculation, using lookup table interpolation], and "1.5 mil Au Solenoid L, Q(f) V4" and "1.0 mil Au Solenoid L, Q(f) V3" [earlier versions]) were coded which calculate values of inductance, L (external inductance, L_{ext}, as well as total inductance, $L_t=L_{ext}+L_{int}(f)$, at frequencies of f=25MHz and 200Mhz are shown in the spreadsheet; L_t is calculated for all frequencies for the Q(f) calculations) and the Q(f) values (at 100 frequency points from f=25MHz to 2.5GHz) for numbers of turns in the circular solenoid from N=1 to N=24 turns (easily extendible to greater numbers of turns). Because EXCEL doesn't support the exotic Kelvin and elliptic integral functions, lookup tables are required in the spreadsheets for M(d/R) for r=R [Eqs. 21 and 22] and for $R_{ac}(f)$ and $L_{int}(f)$ [Eqs. 61 and 62], with the values for these tables originally generated from "HiQ" calculations (Listing 2 and Figure 29). The M(d/R) for r=R lookup table, "R=r=1 Mutual Inductance vs d", is the same for and wire diameter or metal composition as, unlike the self-inductance, the mutual inductance between loops is not a function of wire diameter. The spreadsheet "1.5 mil Al Solenoid L, Q(f) V2" is the latest version of the calculation, using interpolation between lookup table points instead of the standard EXCEL lookup function for better accuracy. $R_{ac}(f)$ and $L_{int}(f)$ are functions of both wire diameter and skin depth, $\delta(f)$, and hence these lookup tables (filenames: "Rac/l for 1.0mil Al,Au&Cu Wires" and "Rac/l for 1.5mil Al & Gold Wire") are specific to the particular wire diameter and metal resistivity chosen for the solenoid inductor design.

Because of the size of these lookup tables, and the fact that the 100 x 24 calculated Q(f, N) data array is already substantial in size, in order to keep the spreadsheet reasonably small, the stacked-loop calculation of the external inductance, L_{ext}, of the solenoid is streamlined in comparison to the full square M_{ij} array used in the "Any S/R Solenoid L Calc v3" spreadsheet. The approach is, given the loop radius, R, and the turns pitch, S, to look up from the "R=r=1 Mutual Inductance vs d" lookup table the mutual inductance values corresponding to the various separations between turns (i.e., M_{12} for d/R=S/R [nearest neighbors], M_{13} for d/R=2S/R [2nd nearest neighbors], M_{14} for d/R=3S/R, M_{15} for d/R=4S/R, etc.). For an N-turn solenoid with constant loop spacing, S/R, there are just N-1 of these discrete mutual inductance values involves in the calculation (e.g., from Eq. 28, all nearest-neighbor mutual inductances are the same [$M_{12}=M_{21}=M_{23}=M_{32}=M_{34}=M_{43}=M_{45}=M_{54}$], all 2nd-nearest neighbor M's are the same, etc.). In addition to these N-1 mutual inductance terms, scaled from the "R=r=1 Mutual Inductance vs d" lookup table by multiplying the R=1 meter table values by the actual loop radius (in meters), the external self-inductance of the loop, L_S (referred to as L_e in Eqs. 23, 25

and 29, but we will term L_S to differentiate it from the external inductance of the whole solenoid, L_{ext}) is calculated from a/R using Eq. 29 (or a more precise value may be pasted in from the "M(r/R) for Spiral Inductors v2C" file for r=R-a (where the values were calculated from Eqs. 21 and 22).

Given the $L_S=L_{1S}=L_{2S}=L_{3S}$... self-inductance value and the N-1 discrete mutual inductance values, the calculation of the solenoid inductance, L_{ext}, is straightforward. For example, simply examining Eq. 28 and counting the equivalent terms gives for this N=5 case

$$L = 5L_S + 2[\, 4M_{12} + 3M_{13} + 2M_{14} + M_{15} \,] \qquad \text{for N=5} \qquad \text{Eq. 63}$$

Clearly, for the general case of N turns,

$$L(N) = NL_S + 2[\, (N-1)M_{12} + (N-2)M_{13} + (N-3)M_{14} + \ldots + M_{1N} \,] \qquad \text{Eq. 64}$$

In the spreadsheet calculations, since the full sequence (N=1, 2, 3 ... 24) of number of turns was desired, the recursive form of Eq. 64 was used,

$$L(N) = L(N-1) + L_S + 2[\, M_{12} + M_{13} + M_{14} + \ldots M_{1N} \,] \qquad \text{Eq. 65}$$

In the Q(f) calculations, the total inductance is used, which is just the external inductance from Eq. 65 plus the length of the wire ($l=2\pi RN$) times the L_i/l internal inductance per meter (Eq. 62; taken from the wire-dependent lookup table in the spreadsheet), with the R_{ac} value obtained from the R_{ac}/l column of the same lookup table in the same way.

Figure 32 shows a plot of the Q(f) for frequencies up to f=2GHz for a circular cylindrical coil, about 84 mils in diameter, of 1.5 mil diameter aluminum wire wound with a 5 mil pitch, for N=1 to 10 turns in the solenoid coil inductor. (The choice of the wire size and wire pitch are for compatibility with the wire sizes and pitches achievable with MCM wirebonding, and the diameter gives the same area as demonstrated for wirebond loops.) At low frequency (up to 50 MHz or so), R_{ac} is nearly constant (see Figure 30a), and L_{ext} (which is the major portion of L) is always independent of frequency, so $Q=2\pi fL/R_{ac}$ is proportional to frequency up to 50Mhz or so. At high frequencies, R_{ac} (Eq. 60), because of the $\sqrt{f}$ dependence of R_S (Eq. 56), varies approximately as $\sqrt{f}$, which leaves Q varying more or less as $\sqrt{f}$, as is clear in Figure 32. It is clear in Figure 32 that the Q increases as the number of turns in the solenoid increases. If there were no mutual inductance between turns, the Q would be independent of the number of turns, N, and be equal to the N=1 curve in Figure 31, because with all $M_{ij}=0$ in Eq. 64 you would have $L=NL_S$, and the wire length is proportional to N, so $R_{ac}=2\pi RN(R_{ac}/l)$, which gives $Q=2\pi fL/R_{ac}=fL_S/[(R_{ac}/l)R]$, which is independent of N. With the mutual inductance coupling between turns added, L in Eq. 64 increases, with no increase in Rac (because the wire length is unchanged), so the Q increases in proportion to $L(N)/NL_S$,

$$Q(N) = Q(N=1)[L(N)/NL_S] \qquad \text{Eq. 66}$$

where L_S=L(N=1). If the coupling between turns were infinitely tight (coefficient of coupling, k=1), that is, $M_{12}=M_{13}=M_{14}=M_{15}...=L_S$, then from Eq. 64 (using the fact that the sum of the first n integers=(n/2)(n+1) with n=N-1 to evaluate the mutual inductance portion of Eq. 64) we would have

$$L(N) = N^2L_S \qquad \text{for } M_{12}=M_{13}=M_{14}...=M_{1N}=L_S \qquad \text{Eq. 67}$$

For this case of infinitely tight turns coupling (completely unrealistic, except with the use of high-permeability cores), we would have from Eqs. 66 and 67,

$$Q(N)/Q(1) = L(N)/NLs = N \qquad \text{for } M_{12}=M_{13}=M_{14}...=M_{1N}=L_S \qquad \text{Eq. 68}$$

Because of the finite turns pitch, S (or more precisely, the pitch to radius ratio, S/R), the mutual inductance between more distant turns in air-core solenoids is much smaller than between nearest-neighbor turns (e.g., in the example of Figure 32, while L_S=5.4575nH, with S/R=0.116912, M_{12}=3.004nH, M_{13}=2.103nH, M_{14}=1.600nH, M_{15}=1.264nH, M_{16}=1.201nH, M_{17}=0.694nH, M_{18}=0.581nH, M_{19}=0.490nH and M_{10}=0.416nH). Hence the increase of inductance, L, with increasing numbers of turns, N, from Eq. 64 falls far below the N^2 dependence of Eq. 67 as the length to radius ratio of the solenoid, NS/R, becomes large. Correspondingly, the increase in Q with increasing numbers of turns, N, slows as NS/R, becomes large, as is quite evident in Figure 32.

Along with the "free Q" that the mutual inductance offers, it also has the advantage of reduced frequency dependence. As the mutual inductance contribution to L increases, the relative contribution of the frequency-dependent internal inductance of the wire conductor becomes relatively smaller. For example, for the coil of Figure 32, with a single turn (N=1), the external inductance is 5.4575nH, while L(200Mhz)=5.6568nH (+3.65%) and L(25MHz)=5.7871nH (+6.04% greater than L_{ext}). With N=4 turns, the external inductance is 9.43x larger than for N=1, 51.467nH, while L(200Mhz)=52.264nH (+1.55%) and L(25Mhz)=52.785nH (+2.56% greater than L_{ext}). In addition to this x2.36 reduction in the change in L with frequency, there is a corresponding increase in Q. For example, at f=200 MHz, Q=23.9 for N=1, while for N=4 turns, Q=55.2 at 200MHz, x2.31 higher. (This factor of x2.31 for Q(4)/Q(1) is exactly that predicted from Eq. 66.)

Figure 33 (derived from the "1.0 mil Al Solenoid L, Q(f) V2" spreadsheet calc) shows the effect of using smaller diameter wire in the coil; 1.0 mil diameter aluminum wire instead of 1.5 mil diameter as in Figure 32. While the turns pitch can be reduced (S=98.2 μm is assumed in Figure 33, as compared to 125 μm in Figure 32), improving the mutual inductances due to the smaller S/R, and L_S is higher because a/R is smaller, the increased L is offset by the larger Rac/l values so the result is lower Q (e.g. for N=4 turns, L=58.57nH and Q(200MHz)=39.04) for 1.0 mil wire.

Calculation of the ac Resistance, R_{ac}, for Substrate Conductor Stripes

In the fabrication of MCM wirebond solenoids, while the top side is created from the wirebond loops, the bottom side of the solenoid is most conveniently implemented with stripes of metallization on the MCM substrate. In order to calculate the Q for such embedded MCM wirebond inductors, we must calculate the ac resistance, R_{ac}/l, of these metal stripe return paths forming the bottom half of the inductors (Eqs. 61 and 62 are used for the wirebond loops on the top half). As was discussed previously, for low frequencies, $\delta >> t_m$ (skin depth >> metal thickness), Eq. 58 is used, while at high frequencies, $\delta << t_m$, for uniform fields Eq. 59 is used. Unfortunately, for the frequency range of interest and the metal thicknesses, t_m, typical for MCMs, usually $\delta \approx t_m$, so neither of these simple approximations works. Fortunately, while this situation is more complicated than the simple asymptotic expressions (Eqs. 58 and 59), it is not as messy as for the round wire case (Eqs. 61 and 62). The case of a thin conductor sheet (or layer on another material) with plane wave incident on <u>one side</u> is treated in E&M texts (e.g., Ramo, Whinnery, and Van Duzer sections 5.19 and 5.20), wherein the surface impedance, R_{sp1}, of a metal plate of thickness, t_m, is found to be, for single-sided conduction,

$$R_{sp1} = R_s \, [\sinh(2t_m/\delta) + \sin(2t_m/\delta)]/[\cosh(2t_m/\delta) - \cos(2t_m/\delta)] \qquad \text{1-Side} \qquad \text{Eq. 69}$$

where R_s (Eq. 56) is the surface resistance of the bulk metal. (Since EXCEL does not have the $\sinh(x)=(e^x-e^{-x})$ and $\cosh(x)=e^x+e^{-x}$) functions, these exponential definitions of the functions are used in the spreadsheet calculations.) In fact, as discussed in conjunction with Figures 24 and 25, and Eq. 53, the substrate stripe conductors in the wirebond solenoid inductors have substantial magnetic field strengths on both sides of the metal "plate". If these fields are equal, then the conduction on both sides will be equal and the center line should be a plane of symmetry, so we should be able to consider the plate as two plates of thickness $t_m/2$ in parallel, each with single-sided conduction as in Eq. 69. Hence, for equal <u>2-sided</u> conduction of a plate of thickness, t_m, we should have

$$R_{sp2} = (R_s/2) \, [\sinh(t_m/\delta) + \sin(t_m/\delta)]/[\cosh(t_m/\delta) - \cos(t_m/\delta)] \qquad \text{2-Sided} \qquad \text{Eq. 70}$$

For a metal stripe of width, w, then the ac resistance per meter is given as

$$R_{ac}/l = R_{sp2}/w \qquad \text{for Equal 2-Sided Conduction} \qquad \text{Eq. 71}$$

When the conduction (H-field) on the two sides of the conductor are somewhat different, the Rac correction factor from Eq. 53 may be used with Eq. 71 as a good approximation, but the "resonance effect", wherein Eq. 69 sometimes gives an R_{sp1} value somewhat lower than the bulk surface resistance, R_s, will presumably not be accurately modeled in this asymmetric conduction case.

The R_{sp1} and R_{sp2} thin plate sheet resistance values (Eqs. 69 and 70) are plotted versus frequency for aluminum in Figure 34, as derived from the spreadsheet calculation "Thin Plate R(Freq) for Al V2". Note that the "resonance effect" never exceeds 8.29% (that is, the single-sided Rsp1 value never drops below 91.71% of R_S, or R_{sp2} is never less than 91.71% of $R_S/2$), so that the fact that this effect may not be modeled well by Eq. 70, particularly for substantially asymmetric current distributions, is not a serious problem. It is important, however, to apply the correction factor from Eq. 53 when the H-fields on the two sides are substantially different. Of course, if virtually all of the H-field is on one side of the conductor, then R_{sp1} (Eq. 69) should be used in Eq. 72 instead of R_{sp2} (i.e., for the given metal thickness, t_m, the upper curve at right side in Figure 34 should be used instead of the lower curve) to calculate R_{ac}.

Calculation of the Q of an MCM Wirebond Solenoid Inductor

The goal of all of this is to develop the capability to predict the performance of MCM embedded inductors. In particular, we are interested in solenoid inductors fabricated using wirebond loop conductors, since these offer much higher performance and lower crosstalk than planar spiral inductors, and there are no CAE tools which handle this structure (as there are for spiral inductors). Figure 35 shows the general structure of an MCM embedded wirebond inductor using substrate metallization returns. (An alternative structure, also investigated by nCHIP, uses low-profile wirebonds for the return path, but unless the substrate metallization is very thin, this structure will have lower Q, as well as lower inductance, than that of Figure 35.) The wire radius, a, substrate metallization stripe width, w, length, l_m, and thickness, t_m, as well as the turns pitch, S, symbols are in agreement with the usage in the various foregoing formulas and technical discussions.

A calculation of the inductance and Q of a wirebond solenoid inductor structure requires, of course, information about the detailed shape of the wirebond loops themselves, since it is this shape which determines the loop area, A_{loop}, and effective radius, R_{eff} (R_{eff} is necessary for the calculation of the self-inductance of the loops, and, through S/R_{eff}, the mutual inductance terms as well), as well as the wire length per turn, l_{wt}, (necessary for the calculation of the internal inductance and ac resistance terms, L_{int} and R_{ac}). Figure 36 shows the extended elliptical shape assumed for the wirebond inductors for the L(N) and Q(f,N) calculations shown in Figures 37 and 38. The wirebond base, l_m=0.330 cm is that taken for the nCHIP first-generation test patterns, and the loop height, 58.5 mils, is based on an average of loop height measurements on 1 mil aluminum wirebonds on a test coupon sent by nCHIP to Mayo. The calculations of A_{loop} (=0.03591 cm^2) and l_{wt} (=0.4805 cm) are shown on Figure 36.

The determination of the effective loop radius, R_{eff}, for this more-or-less semicircular wirebond loop shape in Figure 36 is not straightforward. There are, in fact, potentially two values needed for R_{eff}: $(R_{eff})_{Ls}$ and $(R_{eff})_{Mij}$. $(R_{eff})_{Ls}$ would be the value of R, which, substituted in the circular loop expressions (Eqs. 21-23 or the "M(r/R) for Spiral Inductors v2C" file [Figure 8]), would give a value for the calculated external self-inductance of the loops equal to the actual self-inductance (as needed for use in L_S in Eqs. 25-28 and 63-68). Similarly, the value of $(R_{eff})_{Mij}$ would be the value of R, which, taken with the actual turns pitch, S, gives a value of $d/R=S/R=S/R_{eff}$ which gives the correct values for the inter-loop mutual inductances, M_{ij}, in Eqs. 21-22 or the "R=r=1 Mutual Inductance vs d" lookup table file [Figure 9]. (These M_{ij} values are needed in Eqs. 26-28 and 63-68 for the calculation of the solenoid inductance.) Precise calculation of these $(R_{eff})_{Ls}$ and $(R_{eff})_{Mij}$ values for the "odd-shaped" (≈half-circle) wirebond loop of Figure 36 would represent a fairly "computationally challenging" problem. Fortunately, by far the strongest factor determining the inductance of solenoids is the area of the loop, A_{loop}, not details of the shape. Hence, for the purposes of this calculation, we have taken for R_{eff}, the value which gives the correct loop area, A_{loop}; that is, we assume

$$(R_{eff})_{Ls} = (R_{eff})_{Mij} = R_{eff} = \mathrm{Sqrt}(A_{loop}/\pi) \qquad \text{Eq. 72}$$

At some point in the future, we will try to obtain precise expressions for $(R_{eff})_{Ls}$ and $(R_{eff})_{Mij}$ for some specific wirebond loop geometry, but the use of Eq. 72 as an approximation for Reff (=0.10692 cm in Figure 36) should be fairly accurate (slightly overestimating the L and Q values for the wirebond solenoids).

While the nCHIP first-generation wirebond solenoid inductor samples used 1 mil diameter aluminum wire on an S=98.2 μm pitch, as noted in conjunction with Figures 32 and 33, the use of a larger, 1.5 mil diameter, wire will give improved Q (even though there is some sacrifice necessary in increased turns pitch, S). For the calculations of Figures 37 and 38, S=125 μm was assumed with $d_W = 2a = 1.5$ mil diameter Al wirebonds forming the loops. With S=0.0125 cm and R_{eff}=0.1069 cm, the pitch to radius ratio is S/Reff=0.1169, the same as shown for the coil in Figure 32, so the L(N) values are essentially the same as shown there (L_{int} is slightly different). An EXCEL 4.0 worksheet, "1.5 mil Al Wirebond L, Q(f) V3", was coded for the calculation of L(N) and Q(f, N) for these MCM embedded wirebond inductors. The external inductance portion is the same as for the coil ("1.5 mil Al Solenoid L, Q(f) V2") case used for Figure 32, only with the ac resistance, R_{ac}, and internal inductance, L_{int}, terms modified to reflect the mixed wire and substrate stripe contributions. For an N-turn wirebond inductor, Rac is given as

$$R_{ac} = N\,[\, l_{wt}\,(R_{ac}/l)_{wire} + l_m\,R_{sp2}/w\,] \qquad \text{Eq. 73}$$

where, as shown with Figures 35 and 36, l_{wt} is the length of the bond wire in one loop and $(R_{ac})_{wire}$ is from Eq. 61 or Figures 30a and 30b. In Eq. 73, l_m is the metal

stripe length, and w its width, and R_{sp2} is the "2-sided conduction" sheet resistance from Eq. 70 or Figure 34. The internal inductance, L_{int}, is handled the same way,

$$L_{int} = N [l_{wt} (L_i/l)_{wire} + l_m R_{sp1}/(2\pi f w)] \qquad \text{Eq. 74}$$

only using Eq. 62 (or Figure 30a) for $(L_i/l)_{wire}$, and we are using $L_i = R_{ac}/\omega$ to obtain the internal inductance for the substrate metal stripe.

Figure 37 shows the inductance at f=200 MHz (black solid curve and data points) and also the external inductance (gray curve) vs. number of turns, N, for N=1 to 24 turns in the MCM wirebond solenoid inductor of Figures 35 and 36. Note that N=4 turns is adequate to achieve an inductance of 52.68 nH. Figure 38 shows the Q(f) for this wirebond inductor structure for a substrate metal thickness of t_m=25 μm for numbers of turns from N=1 to 10. The behavior of the Q(F, N) curves in Figure 38 is generally the same as for the wire coil, as discussed in association with Figure 32 (Eqs. 66-68), except that the Q values are higher. For example, for N=4, the wirebond solenoid gives Q(200 MHz)=58.18 or Q(1 Ghz)=135.8, whereas the circular coil of the same 1.5 mil Al wire gave, for N=4, Q(200 MHz)=55.19 or Q(1 Ghz)=133.17. The higher Q values are because the ac resistance of the w=100 μm substrate aluminum stripe is lower than that of the d_W=2a=38.1 μm diameter Al wire, more than offsetting the longer conductor path length that the wirebond inductor has for the same R_{eff}. Note that due to the approximations associated with Eq. 72, and the fact that we have not included the small current non-uniformity correction for the substrate stripes (Eqs. 52 and 53), the values of L and Q calculated here will be slightly high, and even more so if there are metal planes (package lids, surrounding substrate ground planes, etc.) in proximity to the inductor (as these reduce inductance, and may increase losses somewhat). In addition, sometimes real metals, due to surface roughness and non-ideality of the deposition approach, give skin-effect losses somewhat greater than calculated from the nominal resistivity of the metal.

With all of these effects, it would be wise to margin the calculated Q value by at least 20% in comparison to the requirements of the real circuit application. For example, for the customer with the requirement for Q_{min}=40 at f=200 MHz in a 47 nH inductor, a calculated Q=50 or higher would be a reasonable target. Since the MCM embedded wirebond structure gives a calculated Q(200 MHz)=55.2 for N=4 turns (L=52.68 nH) this should be more than adequate to meet the customer's requirements. In fact, note that we actually have substantially more Q than required to meet the customer's needs. Further, of the 200 MHz ac resistance of R_{ac}=1.141Ω, the majority, $(R_{ac})_{wire}$=0.851Ω, comes from the wire, and only $(R_{ac})_{stripe}$=0.290Ω comes from the t_m=25 μm thick by w=100 μm wide substrate stripe. Hence, there would appear to be ample opportunity to save money in the MCM process by reducing the substrate aluminum metallization thickness from 25 μm to a value more compatible with standard MCM processing.

Standard MCM-D fab lines typically use fairly thin metal planes for their interconnects (e.g., standard nCHIP processes use aluminum thicknesses varying from 1 μm to 3 μm). A number of these layers could be used in parallel to increase the effective thickness of sputtered aluminum, but going to a 25 μm metal thickness would require fairly major additions to the process which would presumably add expense. Because of the frequency dependence of the skin depth, δ, the selection of an adequate value for metal thickness, t_m, will be strongly dependent on operating frequency. What we would like is a quantitative evaluation of what metal layer thickness, t_m, would be adequate for the substrate return path stripes in wirebond solenoid inductors to achieve a given Q value at a given frequency. The spreadsheet calculation described above is capable of providing this information. As an illustration of this capability, the "1.5 mil Al Wirebond L, Q(f) V3" spreadsheet was duplicated using different metal thicknesses for the metal plate impedance lookup table [obtained from the "Thin Plate R(f), L(f) for Al V2" spreadsheet]. The results for the wirebond solenoid structure of Figures 35 and 36 for substrate aluminum layer thicknesses of t_m=1.5 μm, 3.0 μm, 6 μm, 9 μm, 12 μm, 15 μm and 25 μm are summarized for f=200 MHz in the "200MHz Q(N) vs Stripe t.Sum" spreadsheet. These results are plotted as Q(200MHz) vs. N in Figure 39. This same data, only for the case of f=950 MHz, is summarized in the "950MHz Q(N) vs Stripe t.Sum", spreadsheet, and is plotted as Q(950MHz) vs. N in Fig. 40.

We can see from Figure 39 that, while at 200 Mhz, t_m=15 μm gives optimum Q, with t_m=12 μm only slightly poorer (<3% lower Q than 15 μm), even thinner metals would suffice to meet the Q(200 MHz)=40 for L=47 nH customer specification cited earlier. Assuming we would need to target a calculated Q=50 to be confident of an actual delivered Q=40, for N=4 turns, t_m=6 μm (calculated Q=46.39) would appear to be a bit too thin, but t_m=9 μm (calculated Q=53.2) should be more than enough metal thickness to meet the specified 200 MHz Q value with this wirebond inductor geometry.

Figure 40 shows the Q(N) at f=950 MHz for this same set of metal thicknesses. Here we see that a metal thickness of t_m=9 μm gives optimum Q (even better than for t_m=15 μm or 25 μm due to the "resonance effect" in Eqs. 69 and 70, discussed in association with Figure 34), but a metal thickness of t_m=6 μm gives calculated Q results almost as good as t_m=9 μm. Because of the questionable accuracy of modeling of the resonance effect by Eq. 70 for asymmetric fields, these t_m=6 μm Q values should probably be margined by 5% or so beyond the usual design margin. In any event, at these higher frequencies, there is no need to have particularly thick substrate metal layers.

While the substrate metallization thicknesses do not, for 200 MHz and higher frequency operation, need to be very thick (e.g., 25 μm is not required), there is no margin for reducing the diameter of the wirebond wire in the solenoid inductors. For example, Figure 41 shows the Q(f) curves for various values of the number of turns, N, from N=1 to 10, for the case of a 1.0 mil aluminum wire diameter (all

curves for t_m=25 μm). Note in Figure 41, for example, that for N=4 turns (L=58.96 nH), the calculated Q(200 MHz) value for the 1.0 mil bondwire is 43.31, less than 75% of the Q(200 MHz) for the 1.5 mil diameter wire case (Figure 38), and not nearly enough to provide suitable design margin for meeting the customer's specification (calculated Q=50 required to insure meeting Q=40 specification). Further, for any given Q, thinner substrate metal can be used with the thicker wirebond wire, for a net cost savings, so going with the thicker bond wire is best. (The use of ribbon bonds in place of round wire wirebond loops could also prove advantageous in some cases).

Accounting for Capacitance Effects on MCM Embedded Inductors

Along with the desired inductance characteristics of MCM wirebond inductors, nature unavoidably brings undesired capacitance effects. I have carried out extensive calculations of the turn-to-turn capacitance for the wirebond solenoid embedded MCM structure of Figure 35. This data, taken along with the turn-by-turn mutual inductance and self-inductance parameters calculated in the various spreadsheets discussed previously, form the basis for quite a detailed ac model for the embedded inductors (e.g., SPICE models). While these detailed models should be quite accurate in predicting the (complex) ac impedance, Z(f), of the embedded inductor structures, it is important to begin with a clear understanding of just what these models imply with regard to the usual parameters quoted for such devices. The parameters most generally quoted are the inductance, L, the self-resonant frequency, f_o (or SRF), the quality factor, Q(f), and the internal capacitance, C_o, of the inductor.

It is important to understand that when a single number such as the internal capacitance, C_o, or self-resonant frequency, f_o, is cited, it is necessarily within the context of a simplified conceptual model of the inductor. The actual frequency-dependent impedance characteristics can be quite complex (particularly for many-turn inductors), containing much more detailed information (e.g., exhibiting multiple resonances, etc.) than can meaningfully be conveyed by only a couple of parameters. Figure 42 shows the simplified model for inductors that is usually assumed when these key inductor parameters are defined. Note that this is a two-terminal model for the inductor, appropriate when the inductor structure is well isolated from ground planes or surrounding circuitry, such that the capacitive (or inductive, for that matter) coupling to other electrodes may be ignored. Note that this is not always the case, and the more complex models we will be generating for SPICE or other circuit simulations can, at least in principle, take these couplings into account. However for these cases with heavy external coupling, the simple parameters like self-resonant frequency, internal capacitance, etc. are in general not uniquely defined (they tend to be dependent on how the inductor structure is connected in the circuit).

The standard simplified model for the isolated inductor in Figure 42 is that of the inductor, L, and its ac series resistance, R_{ac}, shunted at the inductor terminals with a lossless internal capacitance, C_o. As noted in conjunction with Eq. 40, for reasonably high values of Q (or correspondingly, low values of R_{ac}), with the inductor shunted at its terminals by an external lossless capacitor of capacitance value, C_{ext}, the resonant frequency, f_r, will be given by

$$f_r = 1/\{2\pi \ \mathrm{Sqrt}[L\,(C_o + C_{ext})]\} \qquad \text{Eq. 75}$$

or the reciprocal of the resonant frequency by

$$1/f_r^2 = 4\pi^2\, L\,(C_o + C_{ext}) \qquad \text{Eq. 76}$$

This straight-line relationship, illustrated in Figure 42, forms the basis for the functional definitions for the basic inductor parameters. (In fact, this is how these parameters are defined/measured on unknown physical inductors using the HP 4342A "Q Meter"). In general, inductors are intended for use at frequencies substantially lower than their self-resonant frequency (SRF), f_o, given by Eq. 75 with $C_{ext}=0$ as

$$f_o = 1/2\pi\sqrt{LC_o} \qquad \text{(SRF)} \qquad \text{Eq. 77}$$

In fact, the simplified inductor model of Figure 42 may be thought of as a second-order approximation to the low-frequency behavior of the real physical inductor (where the first-order approximation would be $Z(f)=R_{ac}+j2\pi fL$).

While this simplified model works very well for (reasonably well isolated) inductors at low-to medium frequencies, at very high frequencies (near, or above, the SRF), all of the complexities of multiple resonances, etc., can make the behavior of real physical inductors more complex than predicted by the simplified model. In most cases this is not a serious problem in the application of the inductors, since they are not normally used in this frequency regime, but it can prove a problem in characterizing the inductors in terms of the parameters of the simplified model. For example, if one were to simply open-circuit the inductor and attempt to measure the SRF in order to obtain C_o from Eq. 77, one might well end up with parameter values that rather poorly characterize the inductor behavior in the frequency range of its intended use. What this means in terms of the $1/f_r^2$ vs. C_{ext} plot in Figure 42 is that while the upper right portion of the straight line (e.g., for $C_{ext} \geq C_1$ in Figure 42) is indeed straight, at much higher frequencies, near the $C_{ext}=0$ axis, there could be very substantial departures form this "straight-line" relationship. Experimentally, this problem is avoided by carrying out all characterization measurements with lossless external capacitance, C_{ext}, values (e.g., C_1 and C_2 in Figure 42) that are large enough so that the measurement frequencies are kept in the well-behaved range of interest. As seen in Figure 42, the use of two (or more) external capacitance values

allows C_O to be obtained directly as the negative intercept of the $1/f_r^2$ vs. C_{ext} plot (and the true inductance, L, value to be obtained using the formula shown in the figure), with the SRF then calculated from Eq. 77.

Note that these techniques, intended for evaluating the parameters of unknown physical inductors, work equally well for the purpose of extracting these basic simplified model parameters (e.g., L, C_O, Q(f) and SRF) from much more detailed composite SPICE models for the devices. A very common problem is that a very detailed device model gets generated (e.g., containing all of the distributed capacitance, mutual inductance, self inductance, etc. information on a turn-to-turn basis), but one is hard pressed to understand from the elegantly detailed model just what the L, C_O, SRF or Q(f) values for the inductor are. One simply runs the inductor model two or more times in SPICE over frequency with fixed capacitor values (e.g., C_1, C_2... in Figure 42) shunting the terminals, using a unit ac current source drive to find the resonant frequencies, f_1, f_2, etc. The values of C_1, C_2, etc. should be selected to keep the resonant frequency values, f_1, f_2..., (and 3dB bandwidth values for Q(f)), within the range of the intended application frequency for the device. The relations described in Figure 42 and Eqs. 75 - 77 are then used to extract the parameters for the simplified inductor model. It is also useful as a comparison, to run the simplified inductor model itself to compare the predicted Z(f) with that simulated from the more detailed model. Quite frequently it will be found that for well-isolated inductors, the simplified inductor model will, with properly derived parameters, give adequate accuracy for Z(f) over the frequency range of interest, such that the use of more computationally intensive and "messy" detailed models can be avoided in practical circuit simulations.

At this point it should be pointed out that these definitions of inductor parameters and the simplified inductor model into which they fit (and in terms of which they are defined) represent a sound second-order model for the frequency dependence of inductors in the low-to-medium frequency regime. Within the framework of this simplified inductor model in Figure 42, the inductor Q is given by

$$Q(f) = 2\pi f\, L/R_{ac} \qquad \text{Eq. 78}$$

Note that this definition of the Q of an inductor having significant internal capacitance is the same as that of Eq. 38, wherein no mention was made of internal capacitance effects, etc. The reason for this is that the basic definitions of Q as noted in Eqs. 33 - 46 are all related to energy storage/energy dissipation or resonant bandwidth factors that are uninfluenced by the presence of lossless shunting capacitors.

The fact that the definition of Q should not depend on the presence of lossless capacitance elements shunting the inductor is clear from a simple circuit example. Consider a comparison between two inductors having the same true inductance, L, and series resistance values, R_{ac}, but with one having no internal shunt capacitance

(C_O=0) and one having a finite lossless capacitance, C_O=C_1in parallel with it. If the intended application of the inductor is to function in a parallel-resonant ("tank") circuit at a resonant frequency f_r=f_2 in Figure 42, then to use the first (C_O=0) inductor in the circuit, a capacitor of value C_{ext}=C_2 is placed in parallel with the terminals of the inductor. To use the second (C_O=C_1) inductor for this same tank circuit function at the same frequency, it would be placed in parallel with a smaller capacitor, of value C_{ext}=C_1-C_2. In either case, the total capacitance (combined internal + external) across the inductor will be the same (C_1), and hence, assuming all the capacitors to be essentially lossless, the resulting circuit bandwidth, and hence (by Eq. 43) the Q, must be the same, just as indicated by Eqs. 39 and 78.

While the internal capacitance, C_O, of an inductor does not directly lead to problems with Q in many applications, the value of the internal capacitance or SRF can dictate whether a given inductor is usable, due to circuit constraints, in a given application. An obvious case would be the tank circuit example above if the intended application required a resonant frequency higher than f_r=f_1 (the self-resonant frequency of the inductor having C_O=C_1 in the example; see Figure 42). While most bandpass filter, and many other, applications of inductors use them in parallel with capacitors of substantial value, this is not always the case, and even when it is, the inductor would be usable only when the value of circuit capacitance required exceeds C_O. Further, for variable-frequency tuned circuit applications where the inductor is operated in parallel with a variable-capacitance element such as a varactor diode, the presence of self-capacitance will reduce the tuning range available for a given varactor capacitance ratio. Hence, in general, it is desirable to have low C_O (or correspondingly, high SRF) for circuit reasons having little to do with Q.

Definition of Geometry for MCM Embedded Spiral Inductor

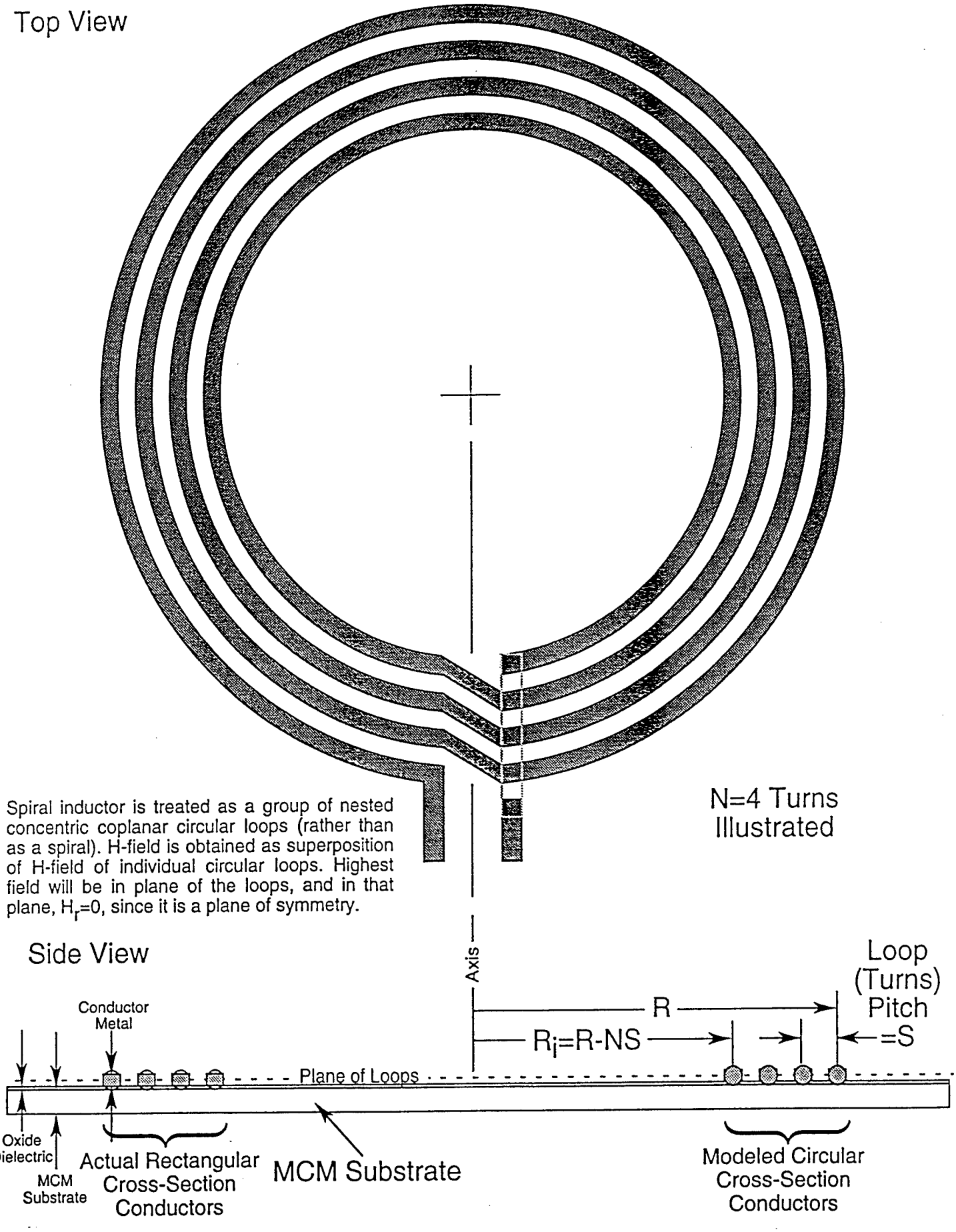


FIGURE 1

Definition of Geometry for Solenoid Magnetic Field Calculation

Solenoid is treated as a stack of parallel circular loops (rather than as a helix). H-field is obtained as superposition of H-field of individual circular loops. Highest field will be in plane of center loop, and in that plane, $H_r=0$ if it is a plane of symmetry, so only odd numbers of loops, N, will be treated for $\overline{H}=H_Z$ plotting.

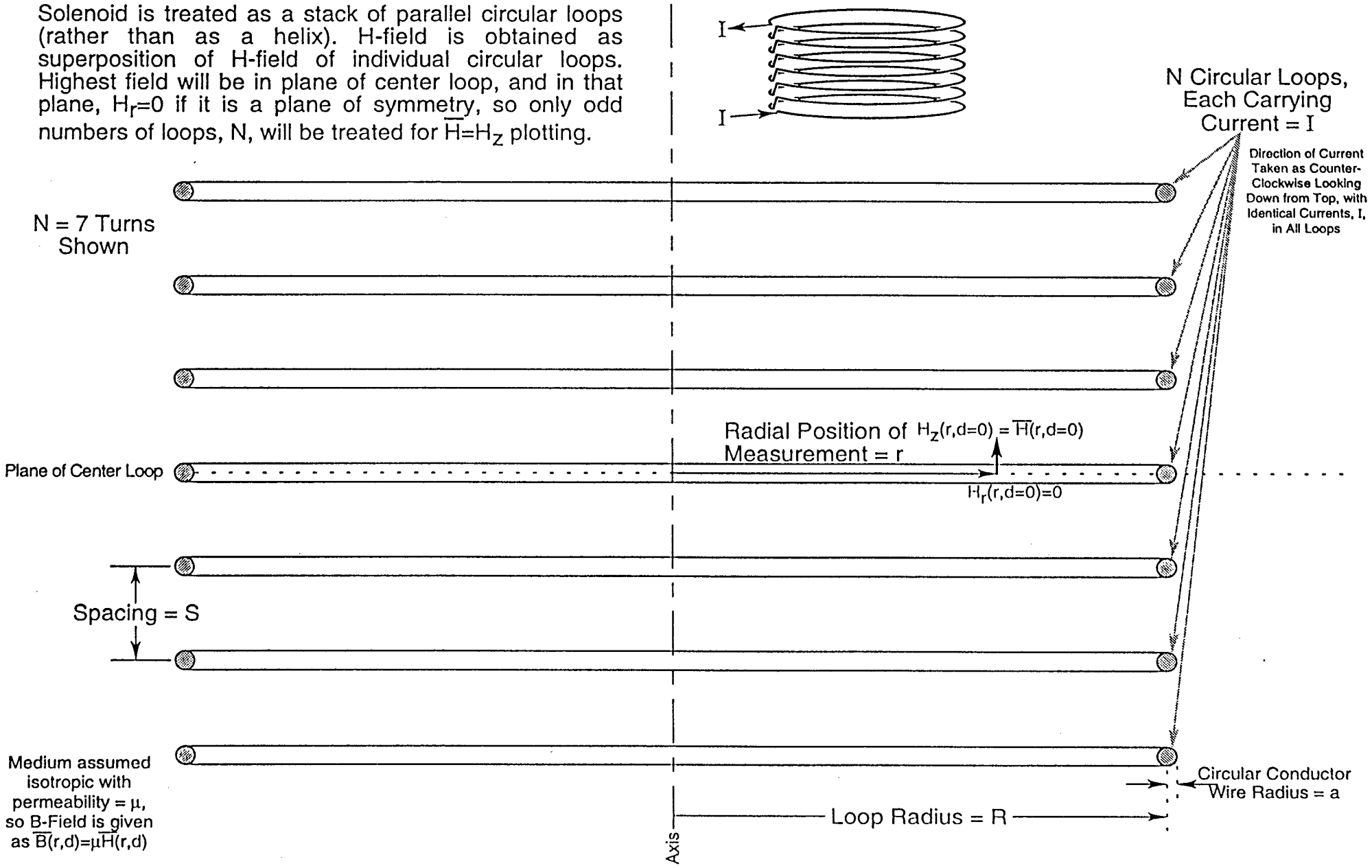


FIGURE 2

Definition of Geometry for Circular Loop Magnetic Field Calculation

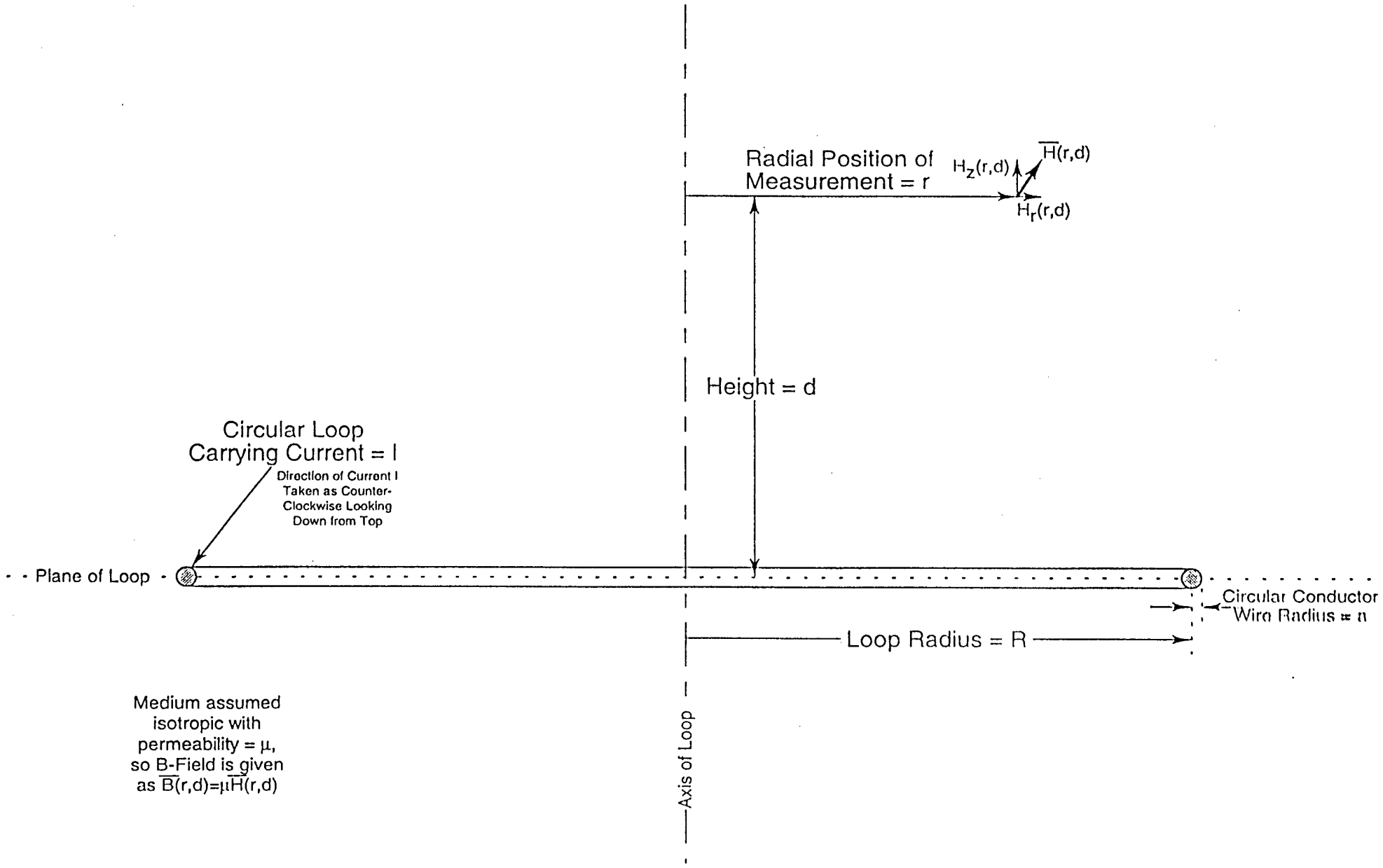


FIGURE 3.

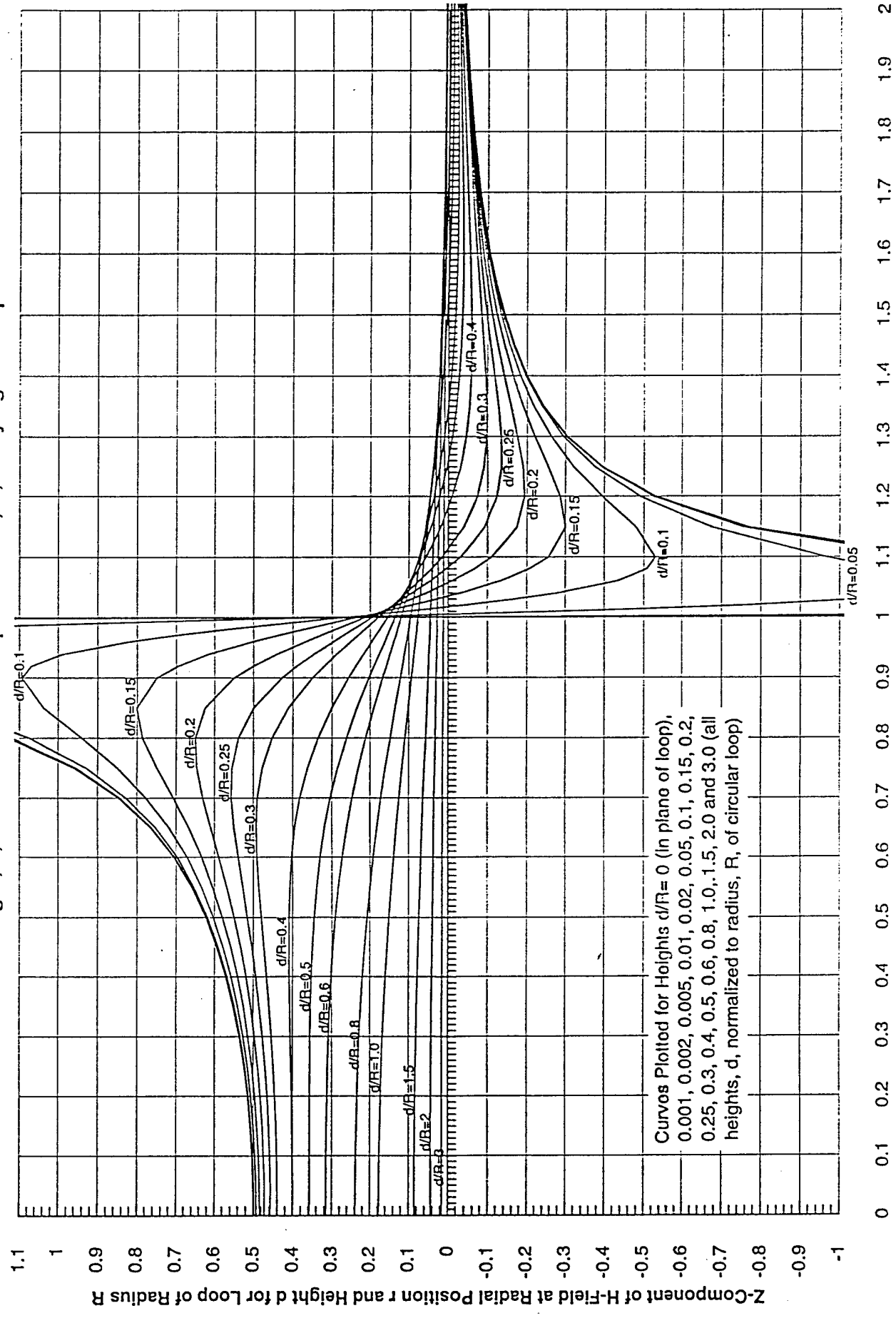

Z-Component of Magnetic Field vs. Radial Position
at Height, d, Above Circular Loop of Radius, R, Carrying I=1 Ampere
Z-Component of H-Field at Radial Position r and Height d for Loop of Radius R
Radius from Axis of Circular Loop at Which H-Field Measured (Norm'd to Radius of Loop, R), r/R
d/R=0.1
d/R=0.15
d/R=0.2
d/R=0.25
d/R=0.3
d/R=0.4
d/R=0.5
d/R=0.6
d/R=0.8
d/R=1.0
d/R=1.5
d/R=2
d/R=3
d/R=0.05
Curves Plotted for Heights d/R= 0 (In plane of loop), 0.001, 0.002, 0.005, 0.01, 0.02, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6, 0.8, 1.0,.1.5, 2.0 and 3.0 (all heights, d, normalized to radius, R, of circular loop)

FIGURE 4.

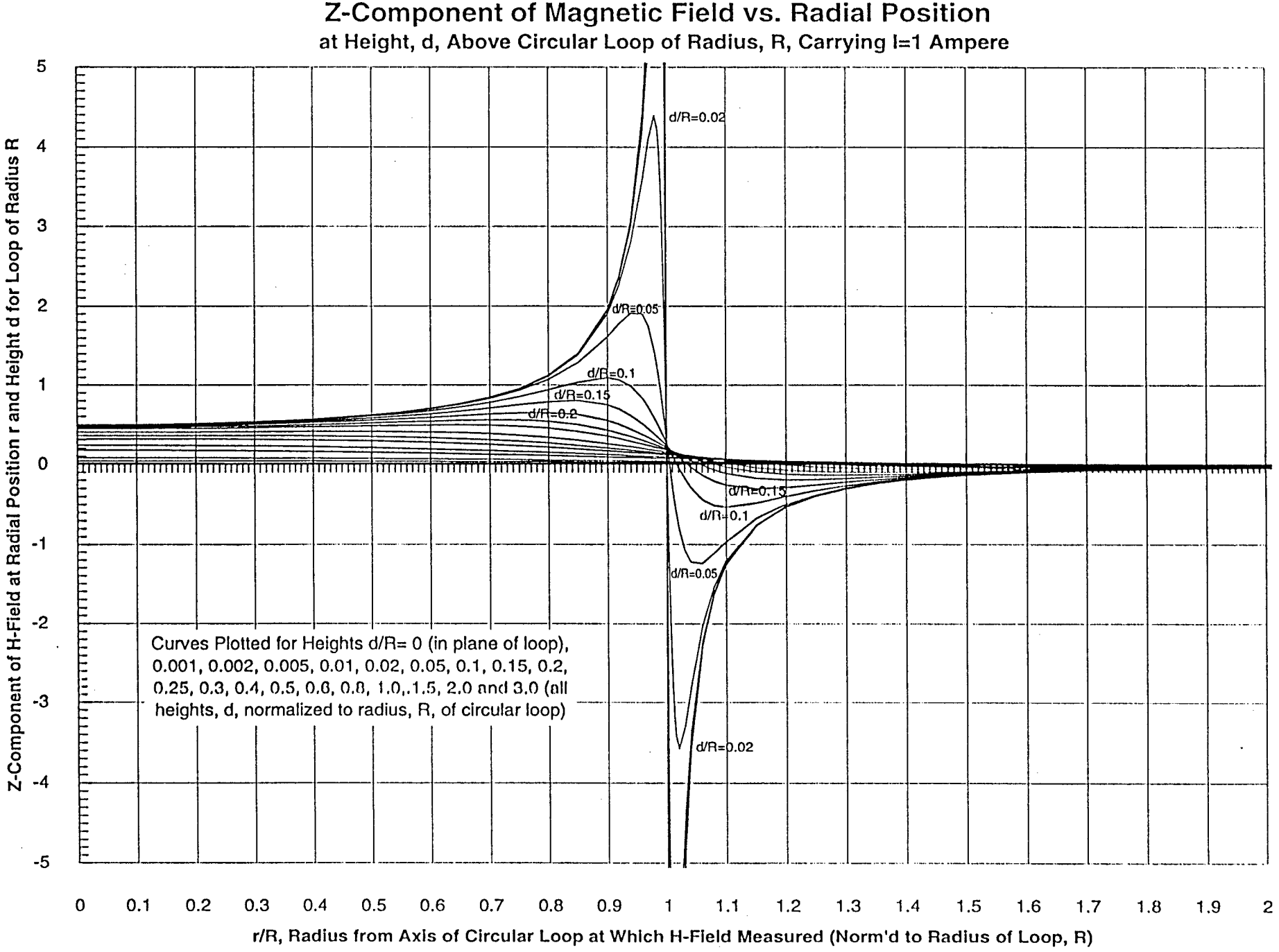

Z-Component of Magnetic Field vs. Radial Position
at Height, d, Above Circular Loop of Radius, R, Carrying I=1 Ampere
Z-Component of H-Field at Radial Position r and Height d for Loop of Radius R
r/R, Radius from Axis of Circular Loop at Which H-Field Measured (Norm'd to Radius of Loop, R)
d/R=0.02
d/R=0.05
d/R=0.1
d/R=0.15
d/R=0.2
Curves Plotted for Heights d/R= 0 (in plane of loop), 0.001, 0.002, 0.005, 0.01, 0.02, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6, 0.8, 1.0,.1.5, 2.0 and 3.0 (all heights, d, normalized to radius, R, of circular loop)

FIGURE 5

Z-Component of Magnetic Field vs. Radial Position

at Height, d, Above Circular Loop of Radius, R, Carrying I=1 Ampere

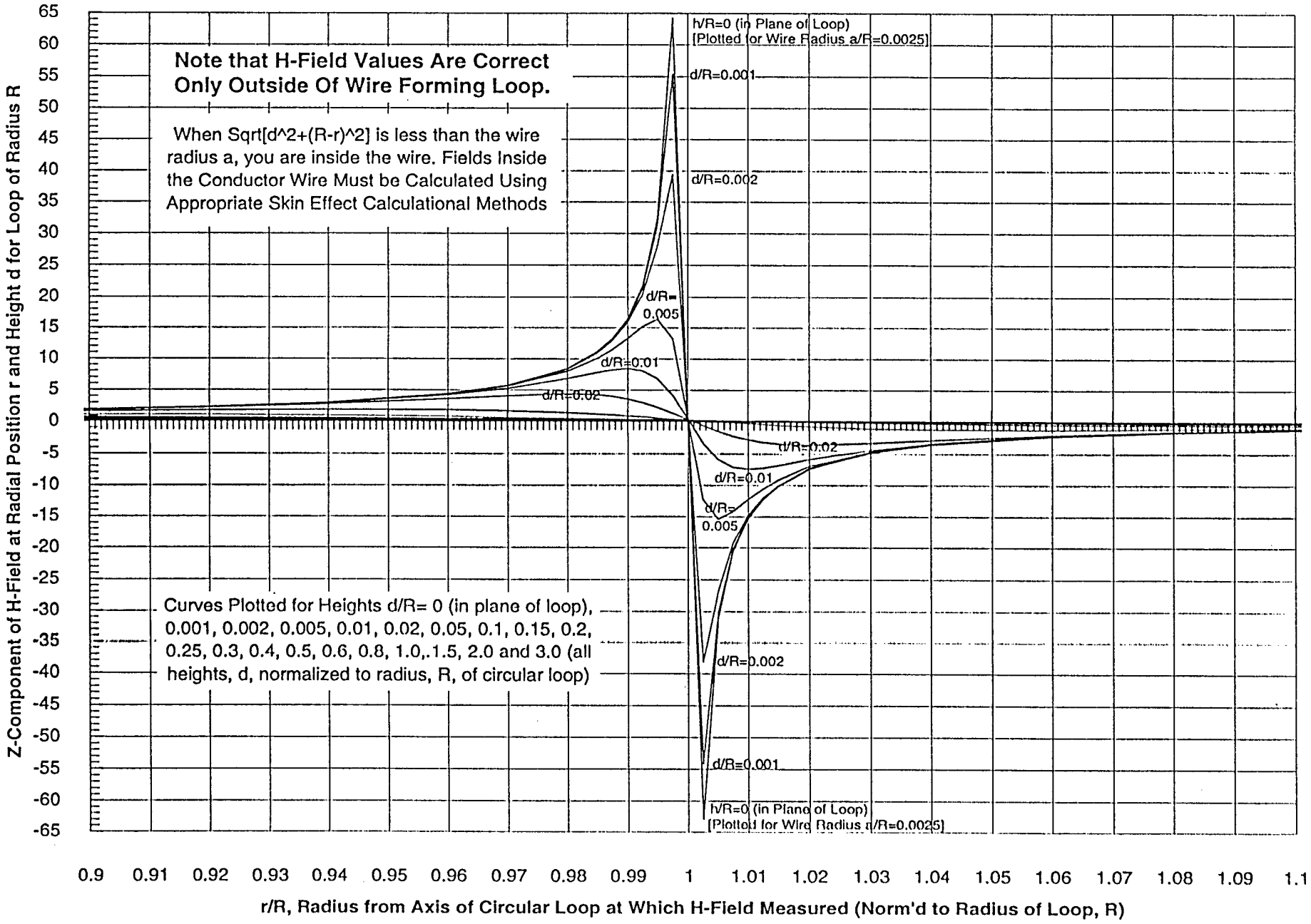


FIGURE 6.

```
// Circular Loop Inductor MutualInductance Calc  R. C. Eden   July 7, 1996
// General calculation set up with d=0 for use with spiral inductors

// Physical Constants: Units are meters, seconds, farads, Henrys, Hz, etc.
pi=3.14159265358979323846;
mu=(4E-7)*pi;                /* Permeability of Free Space in Henries/meter */
clt=2.99792458E8;                 /* Speed of Light in m/s */
Eo=1/(mu*clt*clt);                /* Permitivity of free space */

// Mutual Inductance Calculation for Spiral Inductors; d=0, vary radius b
a=1;                /* Radius of 1st loop in meters */
d=0.0;              /* Height of 2nd loop above 1st loop in meters */
bstep=0.1;          /* Step size on b in meters */
b=0;                /* Initial Value  of radius b in meters */

for i=1 to 9 do
 b=0.0+i*bstep;

ksq=(4*a*b)/(d^2+((a+b)^2));
k=Sqrt(ksq);   /*In HiQ argument of fn is called k instead of k^2 as in texts
Kfn = comel1(ksq);          /* Complete Elliptic Integral of the First Kind */
Efn = comel2(ksq);          /* Complete Elliptic Integral of the Second Kind *
M = mu*Sqrt(a*b)*((((2/k)-k)*Kfn)-((2/k)*Efn));
// Barr[i]=b;
// Marr[i]=M;
BMarr[i,1]=b;
BMarr[i,2]=M;

end for;

//* Note that HiQ uses Abromiwitz and Stegun definition of the  K(k) & E(k)
// Complete Elliptic Integral functions in which k^2 is the modulus
// or argument of the function, instead of k,as in the older Jahnke and Emde
// "Tables of Functions" forms for K(k) and E(k), (as used in Ramo, Whinnery,
// and Van Duzer and most other E&M texts), so in HiQ we must square
// the argument (modulus) of the function first, before calling the functions

// This HiQ Script file Calculates the Mutual Inductance Between Two Circular
// Loops which are Co-Axial, but may be displaced by a height, d, between the
// The Radii of the two loops are "a" and "b" (dimensions in meters)
// For the case of a spiral inductor, the loops are coplanar, so d=0
```

LISTING 7

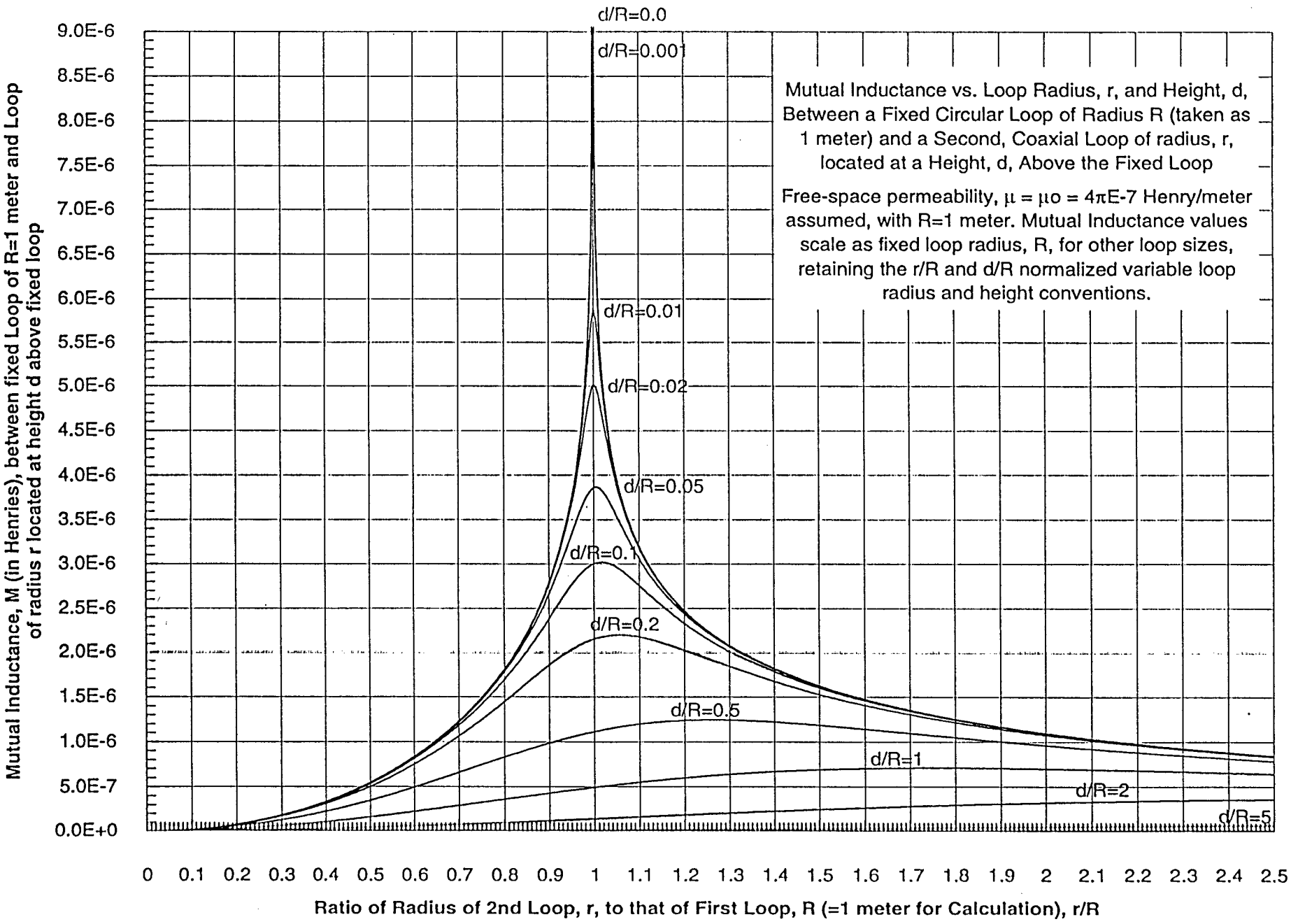
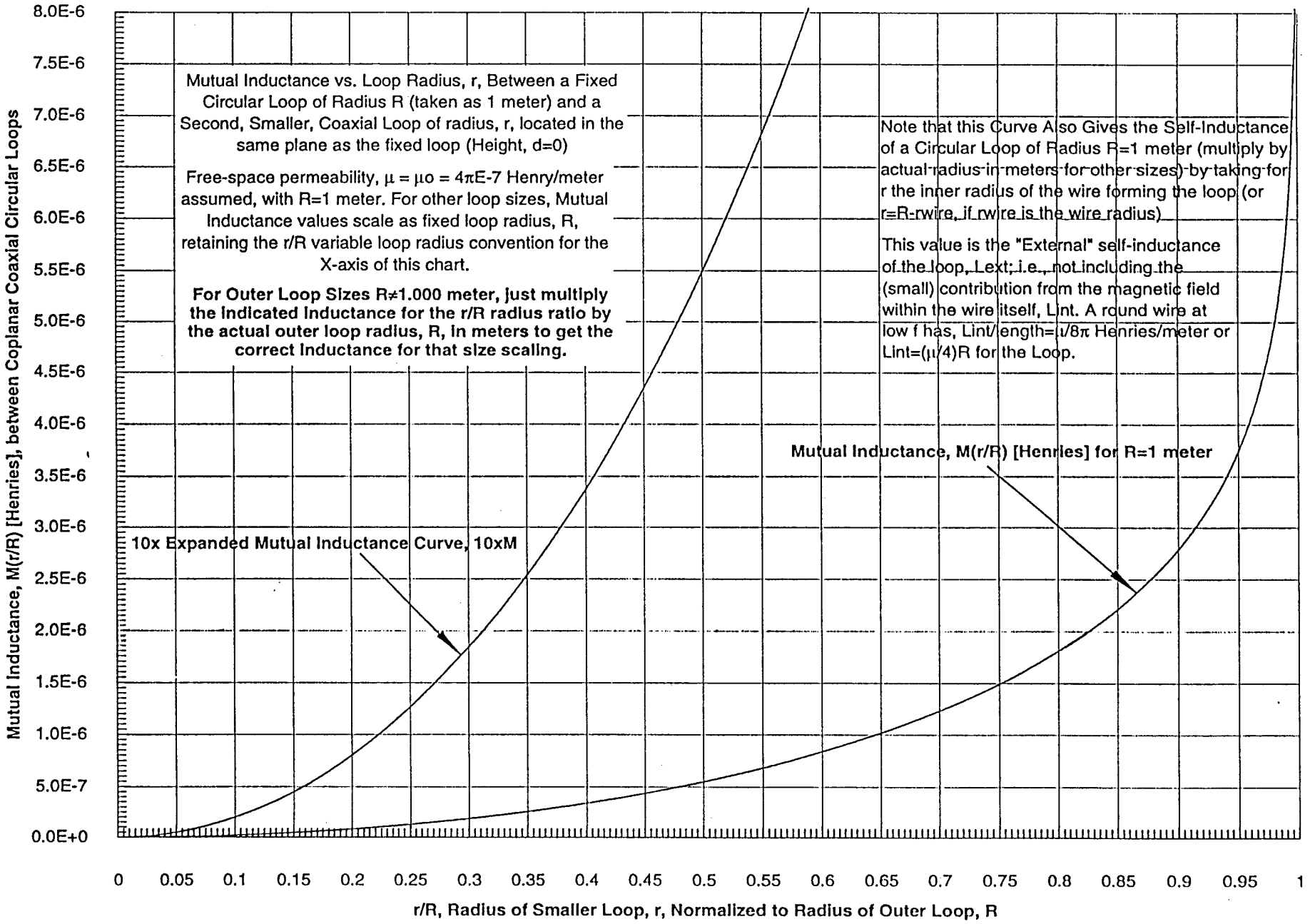

Mutual Inductance Between Coaxial Circular Loops vs. Radius and Height
Mutual Inductance, M (in Henries), between fixed Loop of R=1 meter and Loop of radius r located at height d above fixed loop
9.0E-6
8.5E-6
8.0E-6
7.5E-6
7.0E-6
6.5E-6
6.0E-6
5.5E-6
5.0E-6
4.5E-6
4.0E-6
3.5E-6
3.0E-6
2.5E-6
2.0E-6
1.5E-6
1.0E-6
5.0E-7
0.0E+0
d/R=0.0
d/R=0.001
d/R=0.01
d/R=0.02
d/R=0.05
d/R=0.1
d/R=0.2
d/R=0.5
d/R=1
d/R=2
d/R=5
Mutual Inductance vs. Loop Radius, r, and Height, d, Between a Fixed Circular Loop of Radius R (taken as 1 meter) and a Second, Coaxial Loop of radius, r, located at a Height, d, Above the Fixed Loop
Free-space permeability, μ = μo = 4πE-7 Henry/meter assumed, with R=1 meter. Mutual Inductance values scale as fixed loop radius, R, for other loop sizes, retaining the r/R and d/R normalized variable loop radius and height conventions.
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2 2.1 2.2 2.3 2.4 2.5
Ratio of Radius of 2nd Loop, r, to that of First Loop, R (=1 meter for Calculation), r/R

FIGURE 7.

Mutual Inductance Between Coaxial, Coplanar (d=0), Circular Loops vs. Radius



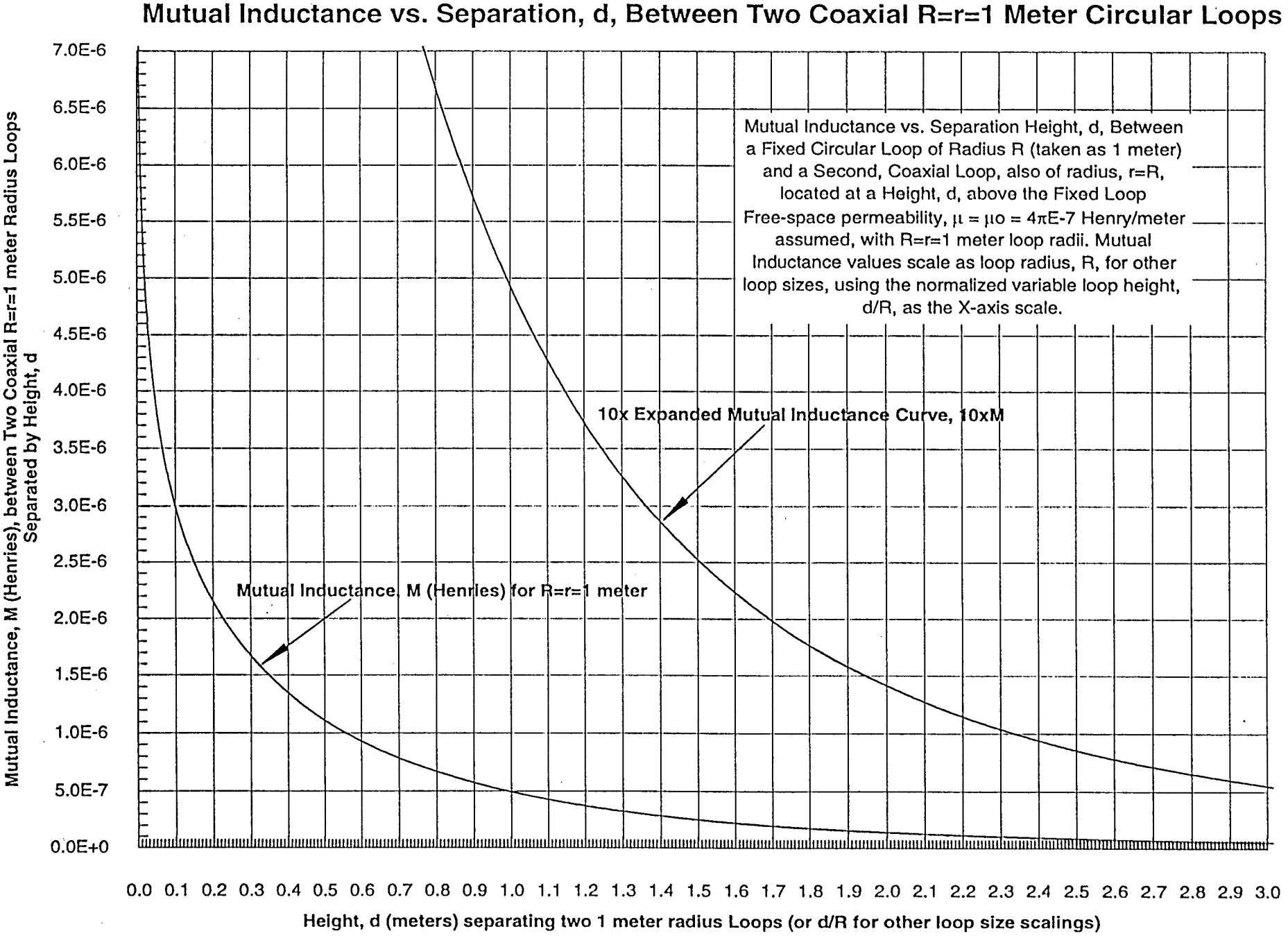

Mutual Inductance vs. Separation, d, Between Two Coaxial R=r=1 Meter Circular Loops
Mutual Inductance, M (Henries), between Two Coaxial R=r=1 meter Radius Loops Separated by Height, d
7.0E-6
6.5E-6
6.0E-6
5.5E-6
5.0E-6
4.5E-6
4.0E-6
3.5E-6
3.0E-6
2.5E-6
2.0E-6
1.5E-6
1.0E-6
5.0E-7
0.0E+0
Mutual Inductance vs. Separation Height, d, Between a Fixed Circular Loop of Radius R (taken as 1 meter) and a Second, Coaxial Loop, also of radius, r=R, located at a Height, d, above the Fixed Loop
Free-space permeability, μ = μo = 4πE-7 Henry/meter assumed, with R=r=1 meter loop radii. Mutual Inductance values scale as loop radius, R, for other loop sizes, using the normalized variable loop height, d/R, as the X-axis scale.
10x Expanded Mutual Inductance Curve, 10xM
Mutual Inductance, M (Henries) for R=r=1 meter
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0
Height, d (meters) separating two 1 meter radius Loops (or d/R for other loop size scalings)

FIGURE 9

```
// Inductance of Thin-Walled Cylindrical Solenoid  R. C. Eden   July 8, 1996
// Using Complete Elliptic Integral formula from Jahnke and Emde page 87.
// L=N^2*(d)*μ*(1/3)*[{(K(k)+((d/l)^2-1)*E(k))/sin(alpha)}-(d/l)^2)]
// Where tan(alpha)=d/l=2R/l, l is length, and k=sin(alpha) is modulus


// Physical Constants: Units are meters, seconds, farads, Henrys, Hz, etc.
pi=3.14159265358979323846;
mu=(4E-7)*pi;                /* Permeability of Free Space in Henries/meter */,
clt=2.99792458E8;               /* Speed of Light in m/s */
Eo=1/(mu*clt*clt);              /* Permitivity of free space */

//Mutual Inductance Calculation
R=1;             /* Radius of Solenoid in meters */
d=2*R;             /* Diameter of Solenoid in meters */
SoverR=0.1;       /* Ratio of turns Spacing, S, to Radius, R */
Nstep=1;      /* Step size on Number of Turns, N */
N=1;             /* Starting Number of Turns */

for i=1 to 50 do
 N=i*Nstep;        /* Number of Turns, N */
 l=N*SoverR;      /* Length of Solenoid, l (meters) */
 alpha=arctan(d/l);
 k=sin(alpha);
 ksq=k*k;     /* Note that HiQ uses Abromiwitz and Stegun definition of the */,
           // Complete Elliptic Integral functions in which k^2 is the modulu
           // or argument of the function, instead of k, so must square k fir
 tanSq=(d/l)^2;
 Kfn = comel1(ksq);          /* Complete Elliptic Integral of the First Kind '
 Efn = comel2(ksq);          /* Complete Elliptic Integral of the Second Kind
 L=(N*N*d*mu/3)*(((Kfn+(tanSq-1)*Efn)/k)-tanSq);   /* Inductance in Henries '
 NLarr[N,1]=N;          /* Store Number of Turns, N, in First Column */
 NLarr[N,2]=L;          /* Store Inductance, L, in Second Column */
 NLarr[N,3]=l;          /* Store Length of Solenoid, l, in Third Column */

end for;


// This HiQ Script file Calculates the Inductance of a Solenoid of Radius R
// and Turns Spacing S (entered as S/R ratio called "SoverR" in HiQ Script
// for 50 values of the number of turns, N, (N=1 to 50) in the solenoid
// Filename = "SoleniodInductanceCalcJEv1p1"
```

Listing 2

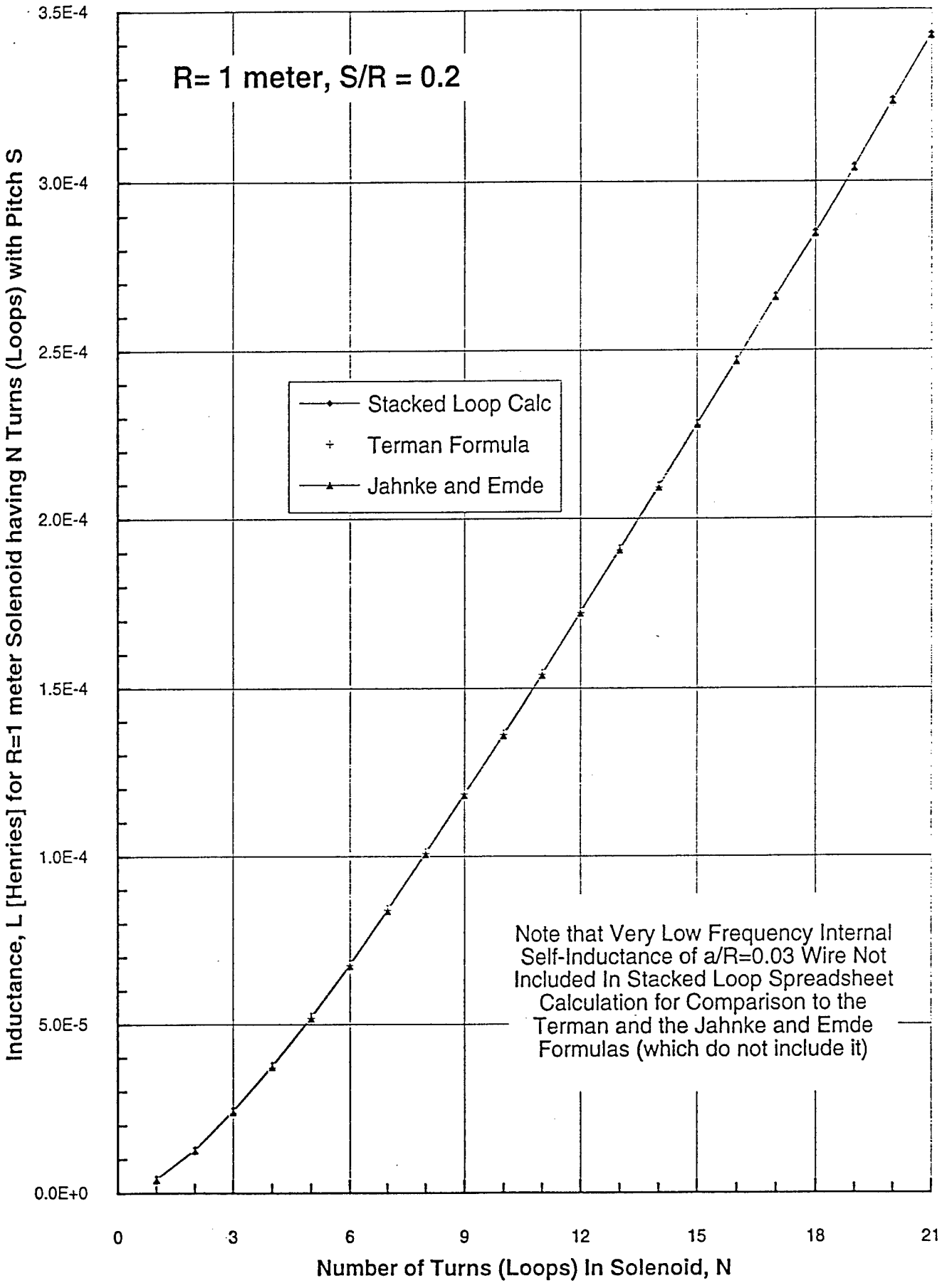

Inductance vs. Number of Turns for Solenoid
R= 1 meter, S/R = 0.2
Stacked Loop Calc
Terman Formula
Jahnke and Emde
Note that Very Low Frequency Internal Self-Inductance of a/R=0.03 Wire Not Included In Stacked Loop Spreadsheet Calculation for Comparison to the Terman and the Jahnke and Emde Formulas (which do not include it)
Inductance, L [Henries] for R=1 meter Solenoid having N Turns (Loops) with Pitch S
3.5E-4
3.0E-4
2.5E-4
2.0E-4
1.5E-4
1.0E-4
5.0E-5
0.0E+0
0
3
6
9
12
15
18
21
Number of Turns (Loops) In Solenoid, N

FIGURE 20.

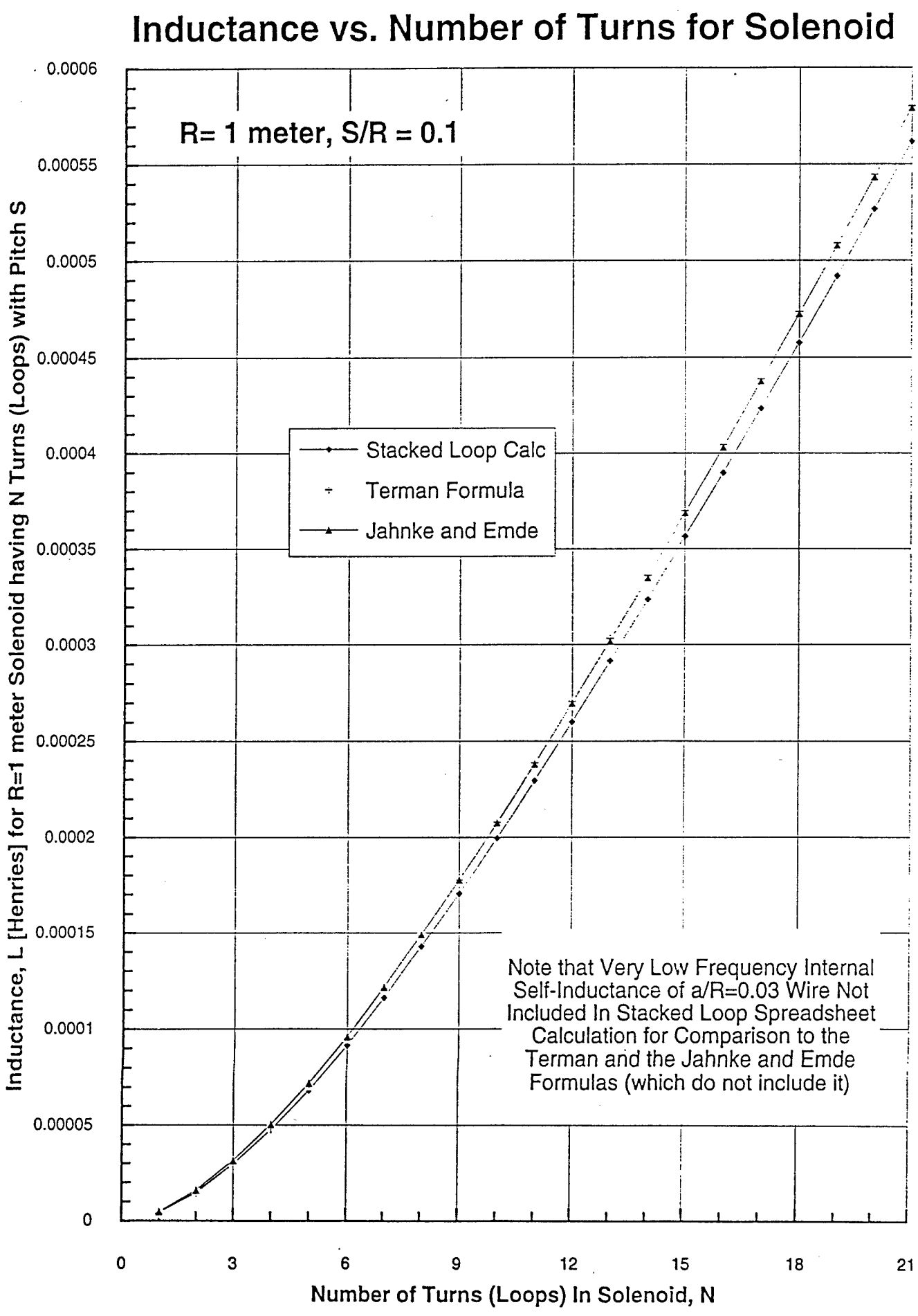

Inductance vs. Number of Turns for Solenoid
R= 1 meter, S/R = 0.1
Stacked Loop Calc
Terman Formula
Jahnke and Emde
Note that Very Low Frequency Internal Self-Inductance of a/R=0.03 Wire Not Included In Stacked Loop Spreadsheet Calculation for Comparison to the Terman and the Jahnke and Emde Formulas (which do not include it)
Inductance, L [Henries] for R=1 meter Solenoid having N Turns (Loops) with Pitch S
0.0006
0.00055
0.0005
0.00045
0.0004
0.00035
0.0003
0.00025
0.0002
0.00015
0.0001
0.00005
0
0
3
6
9
12
15
18
21
Number of Turns (Loops) In Solenoid, N

FIGURE 11.

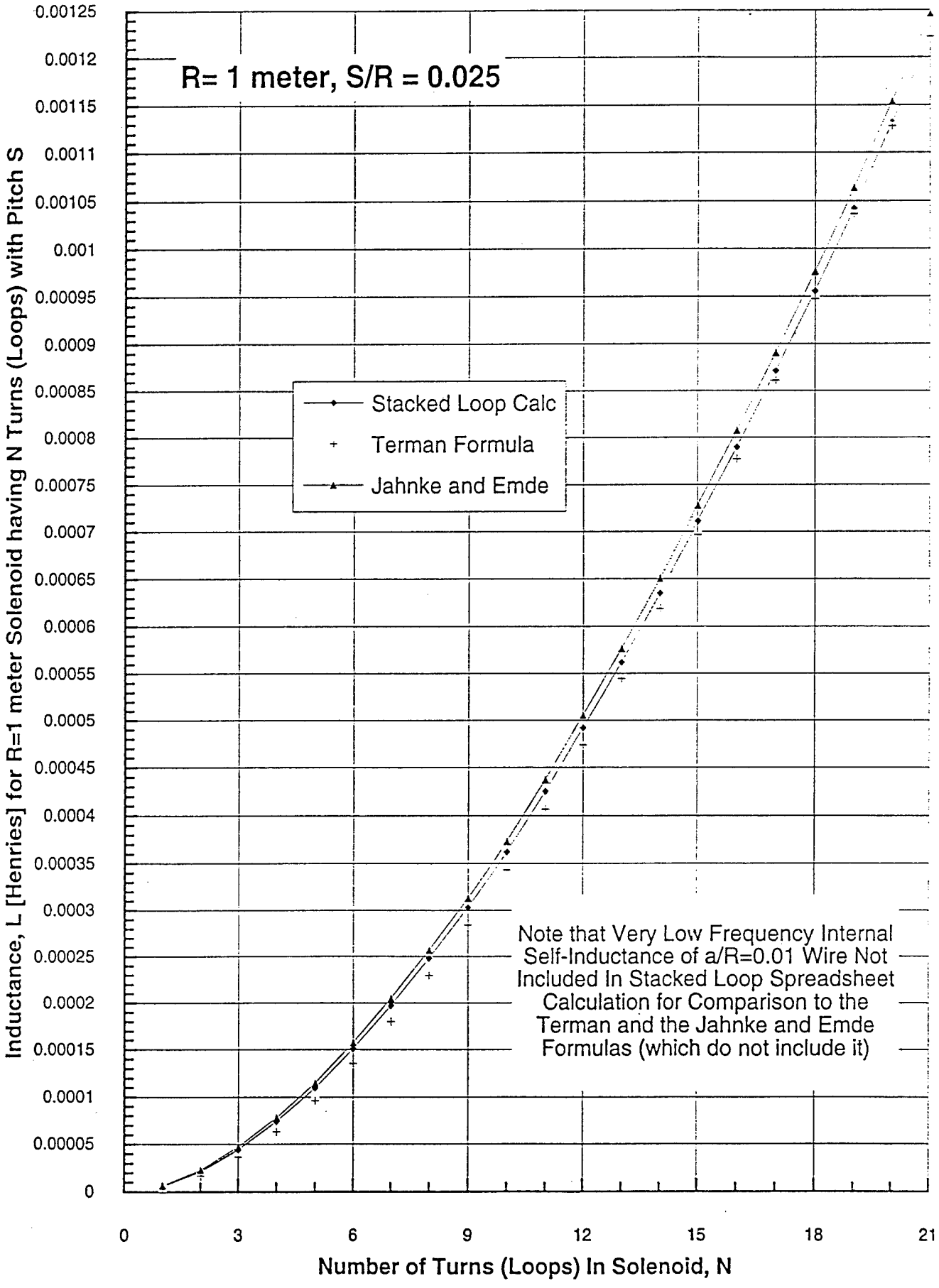

Inductance vs. Number of Turns for Solenoid
R= 1 meter, S/R = 0.025
Stacked Loop Calc
Terman Formula
Jahnke and Emde
Note that Very Low Frequency Internal Self-Inductance of a/R=0.01 Wire Not Included In Stacked Loop Spreadsheet Calculation for Comparison to the Terman and the Jahnke and Emde Formulas (which do not include it)
Inductance, L [Henries] for R=1 meter Solenoid having N Turns (Loops) with Pitch S
0.00125
0.0012
0.00115
0.0011
0.00105
0.001
0.00095
0.0009
0.00085
0.0008
0.00075
0.0007
0.00065
0.0006
0.00055
0.0005
0.00045
0.0004
0.00035
0.0003
0.00025
0.0002
0.00015
0.0001
0.00005
0
0
3
6
9
12
15
18
21
Number of Turns (Loops) In Solenoid, N

FIGURE 12a

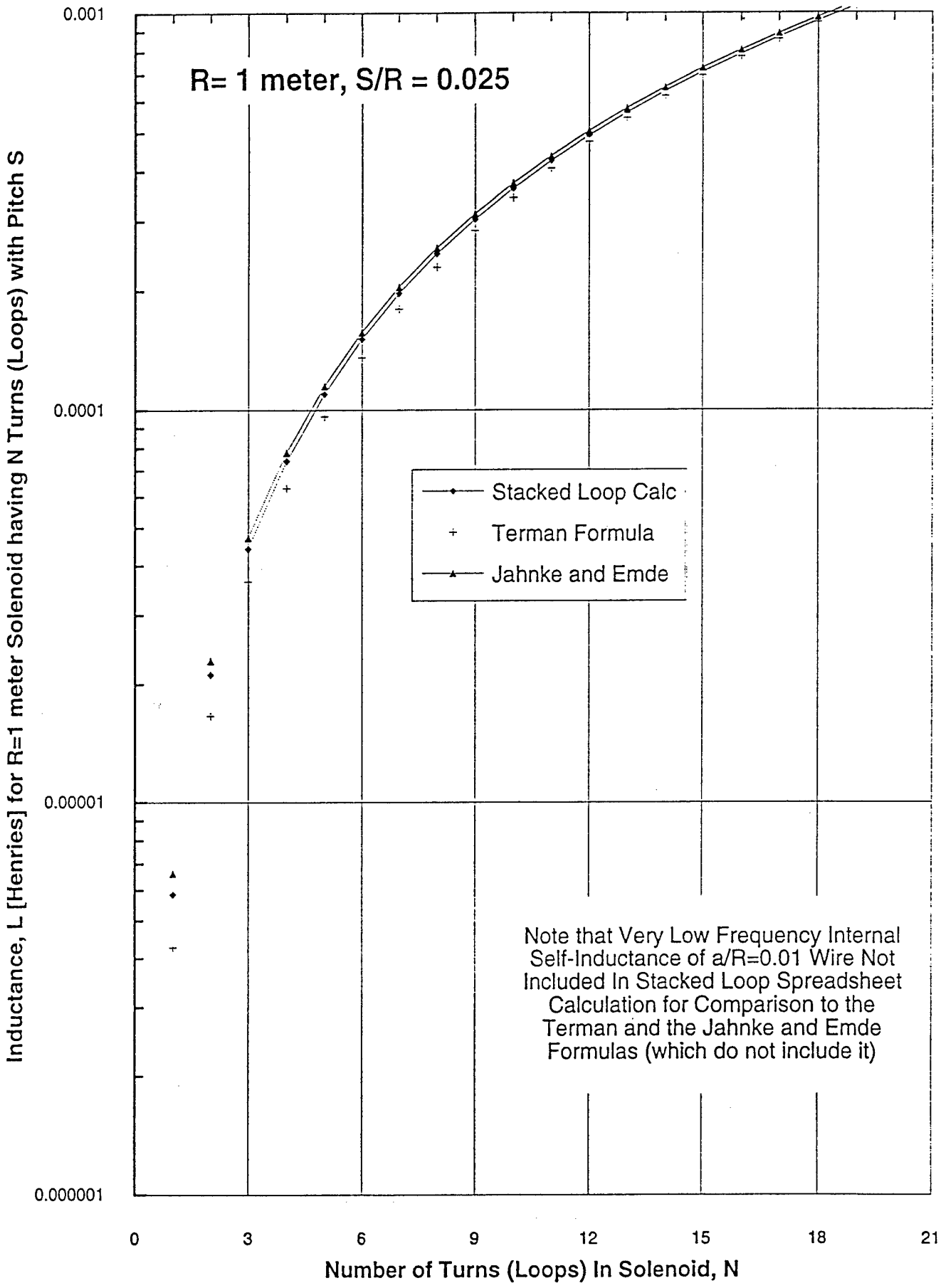

Inductance vs. Number of Turns for Solenoid
R= 1 meter, S/R = 0.025
Inductance, L [Henries] for R=1 meter Solenoid having N Turns (Loops) with Pitch S
0.001
0.0001
0.00001
0.000001
Stacked Loop Calc
Terman Formula
Jahnke and Emde
Note that Very Low Frequency Internal Self-Inductance of a/R=0.01 Wire Not Included In Stacked Loop Spreadsheet Calculation for Comparison to the Terman and the Jahnke and Emde Formulas (which do not include it)
0
3
6
9
12
15
18
21
Number of Turns (Loops) In Solenoid, N

FIGURE 12b.

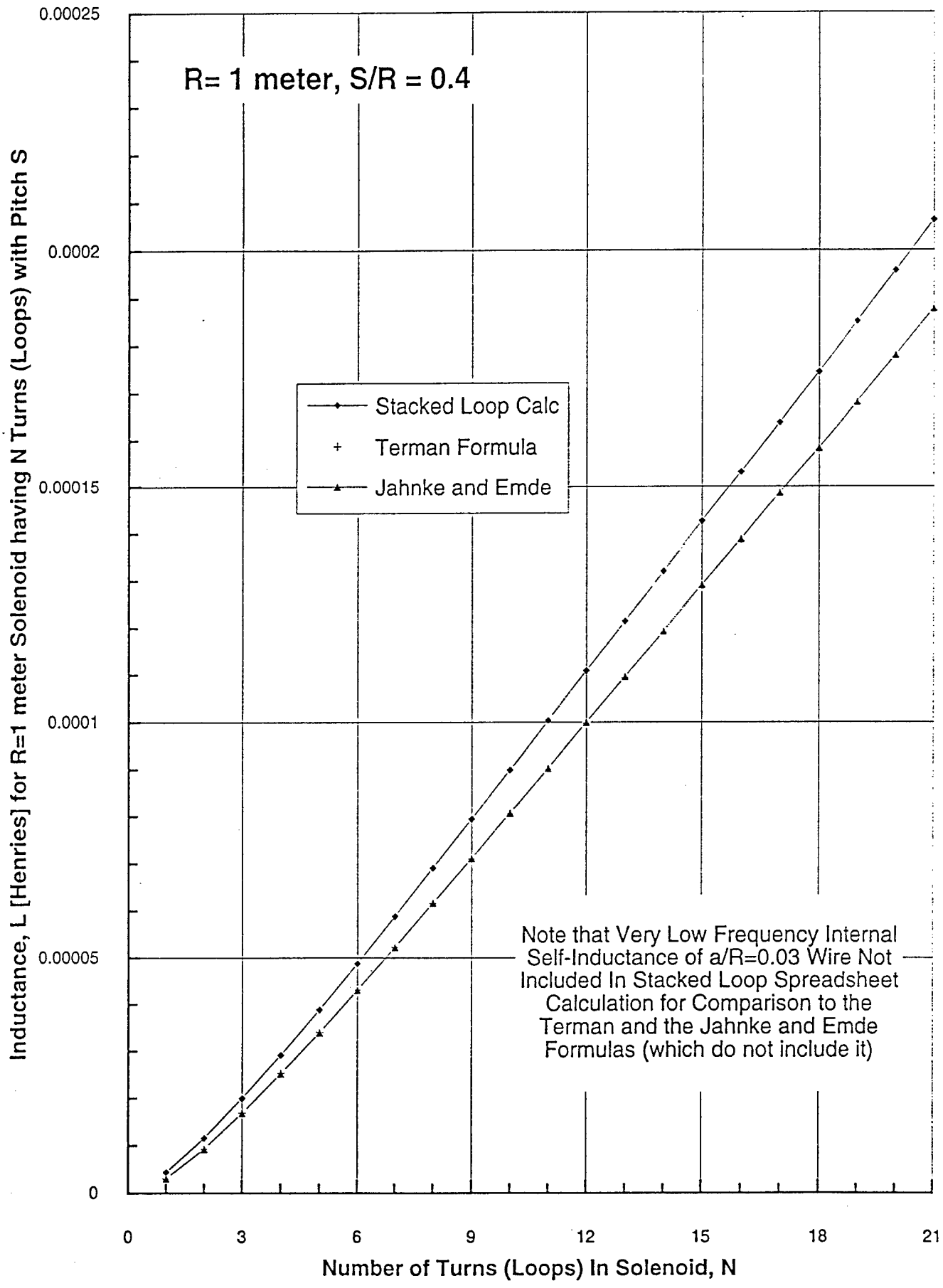

Inductance vs. Number of Turns for Solenoid
R= 1 meter, S/R = 0.4
Stacked Loop Calc
Terman Formula
Jahnke and Emde
Note that Very Low Frequency Internal Self-Inductance of a/R=0.03 Wire Not Included In Stacked Loop Spreadsheet Calculation for Comparison to the Terman and the Jahnke and Emde Formulas (which do not include it)
Inductance, L [Henries] for R=1 meter Solenoid having N Turns (Loops) with Pitch S
0.00025
0.0002
0.00015
0.0001
0.00005
0
0
3
6
9
12
15
18
21
Number of Turns (Loops) In Solenoid, N

FIGURE 13.

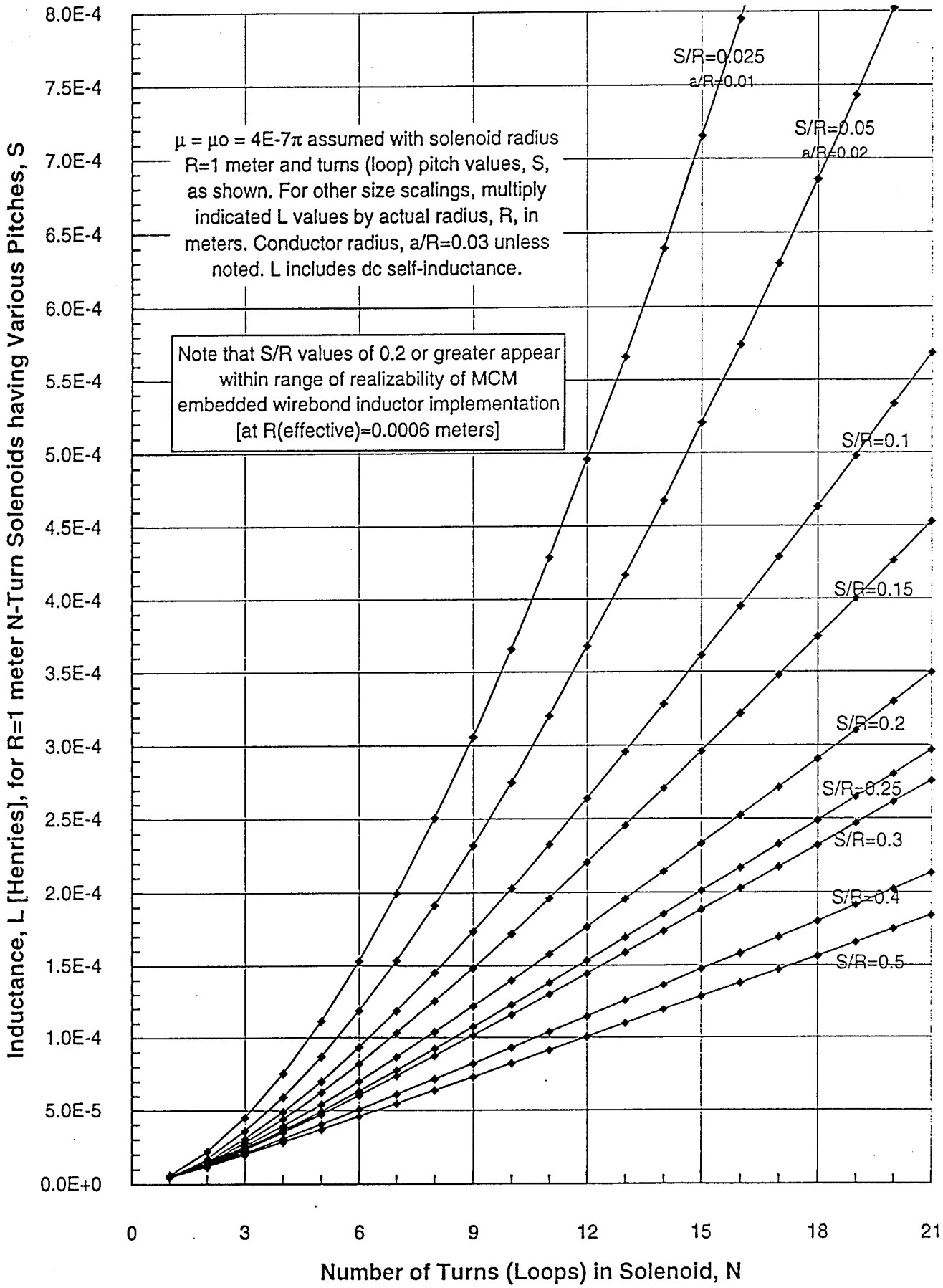

Inductance vs. Number of Turns for R=1 meter Solenoids with Various Pitches, S/R
Inductance, L [Henries], for R=1 meter N-Turn Solenoids having Various Pitches, S
8.0E-4
7.5E-4
7.0E-4
6.5E-4
6.0E-4
5.5E-4
5.0E-4
4.5E-4
4.0E-4
3.5E-4
3.0E-4
2.5E-4
2.0E-4
1.5E-4
1.0E-4
5.0E-5
0.0E+0
0
3
6
9
12
15
18
21
Number of Turns (Loops) in Solenoid, N
μ = μo = 4E-7π assumed with solenoid radius R=1 meter and turns (loop) pitch values, S, as shown. For other size scalings, multiply indicated L values by actual radius, R, in meters. Conductor radius, a/R=0.03 unless noted. L includes dc self-inductance.
Note that S/R values of 0.2 or greater appear within range of realizability of MCM embedded wirebond inductor implementation [at R(effective)≈0.0006 meters]
S/R=0.025
a/R=0.01
S/R=0.05
a/R=0.02
S/R=0.1
S/R=0.15
S/R=0.2
S/R=0.25
S/R=0.3
S/R=0.4
S/R=0.5

FIGURE 14.

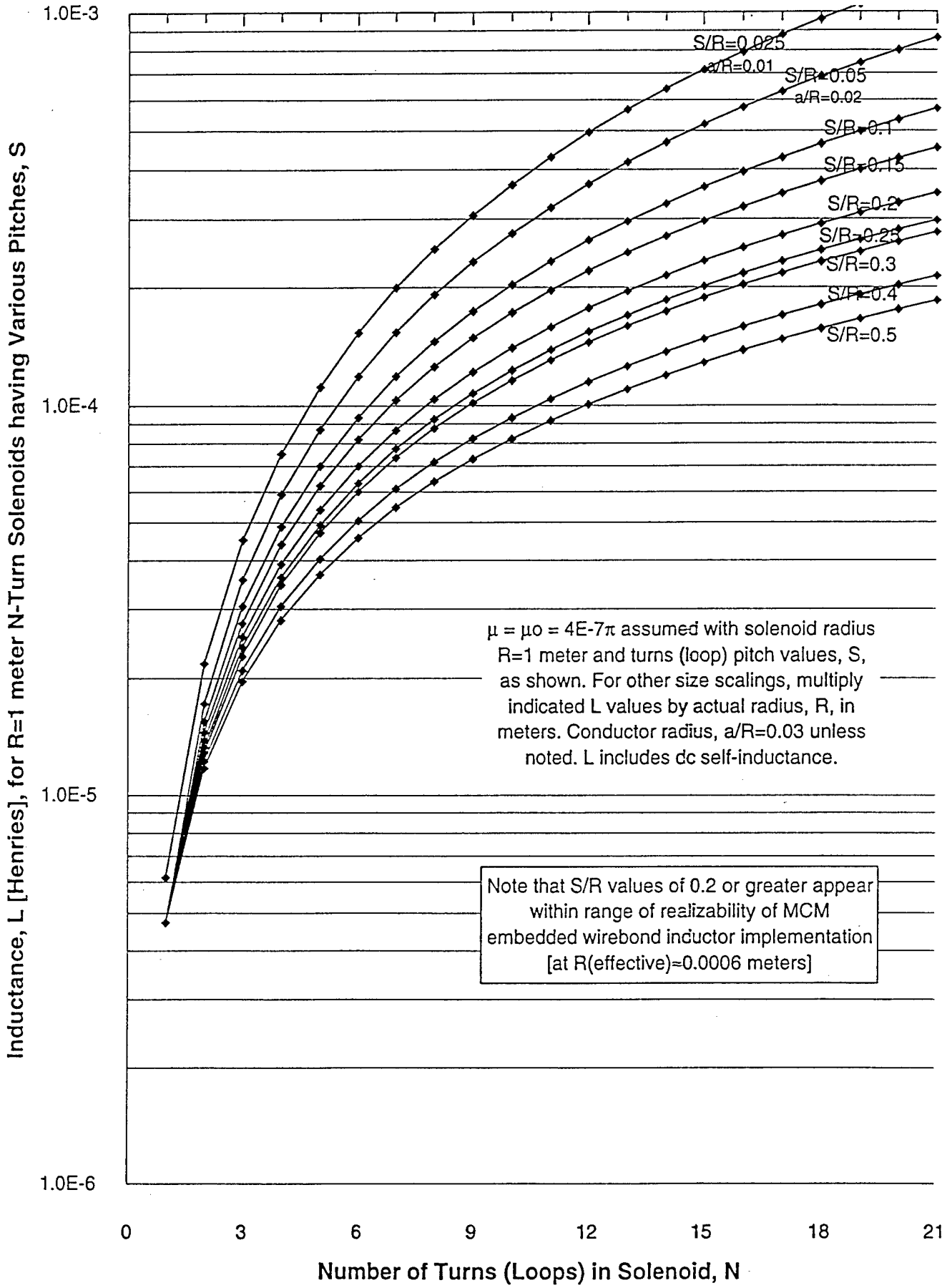

Inductance vs. Number of Turns for R=1 meter Solenoids with Various Pitches, S/R
1.0E-3
1.0E-4
1.0E-5
1.0E-6
Inductance, L [Henries], for R=1 meter N-Turn Solenoids having Various Pitches, S
0
3
6
9
12
15
18
21
Number of Turns (Loops) in Solenoid, N
S/R=0.025
a/R=0.01
S/R=0.05
a/R=0.02
S/R=0.1
S/R=0.15
S/R=0.2
S/R=0.25
S/R=0.3
S/R=0.4
S/R=0.5
μ = μo = 4E-7π assumed with solenoid radius R=1 meter and turns (loop) pitch values, S, as shown. For other size scalings, multiply indicated L values by actual radius, R, in meters. Conductor radius, a/R=0.03 unless noted. L includes dc self-inductance.
Note that S/R values of 0.2 or greater appear within range of realizability of MCM embedded wirebond inductor implementation [at R(effective)≈0.0006 meters]

FIGURE 15

Summary of R=1 meter Solenoid L vs N Data, Including Very Low Frequency Internal Self-Inductance

Richard C. Eden 7/14/96

S/R=	0.5	0.4	0.3	0.25	0.2	0.15	0.1	0.05	0.025
a/R=	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.02	0.01
N=									
1	4.73463E-06	4.73463E-06	4.73463E-06	4.73463E-06	4.73463E-06	4.73463E-06	4.73463E-06	4.73463E-06	6.16537E-06
2	1.16945E-05	1.21707E-05	1.28193E-05	1.3245E-05	1.3777E-05	1.44755E-05	1.5475E-05	1.72036E-05	2.18032E-05
3	1.96425E-05	2.09435E-05	2.27632E-05	2.39805E-05	2.55208E-05	2.75663E-05	3.05231E-05	3.56783E-05	4.51753E-05
4	2.8096E-05	3.04624E-05	3.45665E-05	3.61634E-05	3.91239E-05	4.40072E-05	4.89212E-05	5.91593E-05	7.52687E-05
5	3.68333E-05	4.04287E-05	4.71158E-05	4.93344E-05	5.40637E-05	6.23074E-05	7.00208E-05	8.69479E-05	0.000111368
6	4.57419E-05	5.06786E-05	6.01706E-05	6.32028E-05	6.99916E-05	8.20549E-05	9.33456E-05	0.000118512	0.000152921
7	5.47604E-05	6.11172E-05	7.3731E-05	7.75768E-05	8.66657E-05	0.00010325	0.00011853	0.000153427	0.00019948
8	6.38531E-05	7.16862E-05	8.75464E-05	9.23256E-05	0.000103913	0.000125364	0.000145284	0.000191339	0.00025067
9	7.29977E-05	8.23486E-05	0.000101551	0.000107358	0.000121608	0.000148224	0.000173375	0.000231954	0.000306167
10	8.21801E-05	9.30797E-05	0.000115743	0.000122609	0.000139656	0.000171831	0.000202611	0.000275015	0.000365691
11	9.13906E-05	0.000103863	0.000130046	0.000138032	0.000157989	0.000195942	0.000232836	0.000320301	0.000428989
12	0.000100623	0.000114686	0.000144435	0.000153591	0.000176551	0.000220476	0.000263917	0.000367618	0.00049584
13	0.000109872	0.000125541	0.00015891	0.00016926	0.000195302	0.000245431	0.000295745	0.000416794	0.000566041
14	0.000119134	0.000136421	0.00017344	0.000185019	0.00021421	0.000270685	0.000328225	0.000467677	0.000639408
15	0.000128408	0.000147322	0.000188017	0.000200851	0.000233247	0.000296194	0.000361279	0.00052013	0.000715774
16	0.00013769	0.00015824	0.000202631	0.000216746	0.000252395	0.000321922	0.000394838	0.00057403	0.000794983
17	0.00014698	0.000169171	0.000217277	0.000232692	0.000271636	0.000347839	0.000428844	0.000629267	0.000876895
18	0.000156275	0.000180115	0.000231949	0.000248683	0.000290957	0.000373919	0.000463248	0.000685741	0.000961375
19	0.000165576	0.000191068	0.000246648	0.000264711	0.000310346	0.000400163	0.000498005	0.00074336	0.001048302
20	0.000174882	0.00020203	0.000261367	0.000280772	0.000329796	0.000426531	0.000533079	0.000802043	0.001137562
21	0.000184191	0.000213	0.000276102	0.000296861	0.000349297	0.00045301	0.000568437	0.000861714	0.001229046

$\mu = \mu o = 4E\text{-}7\pi$ assumed with solenoid radius R=1 meter and turns (loop) pitch values, S, as shown.
For other size scalings, multiply indicated L values by actual radius, R, in meters.
Conductor radius, a/R=0.03 unless noted. L includes dc self-inductance.

Note that S/R values of 0.2 or greater appear within range of realizability of MCM embedded wirebond inductor implementation [at R(effective)≈0.0006 meters]

Table 1.

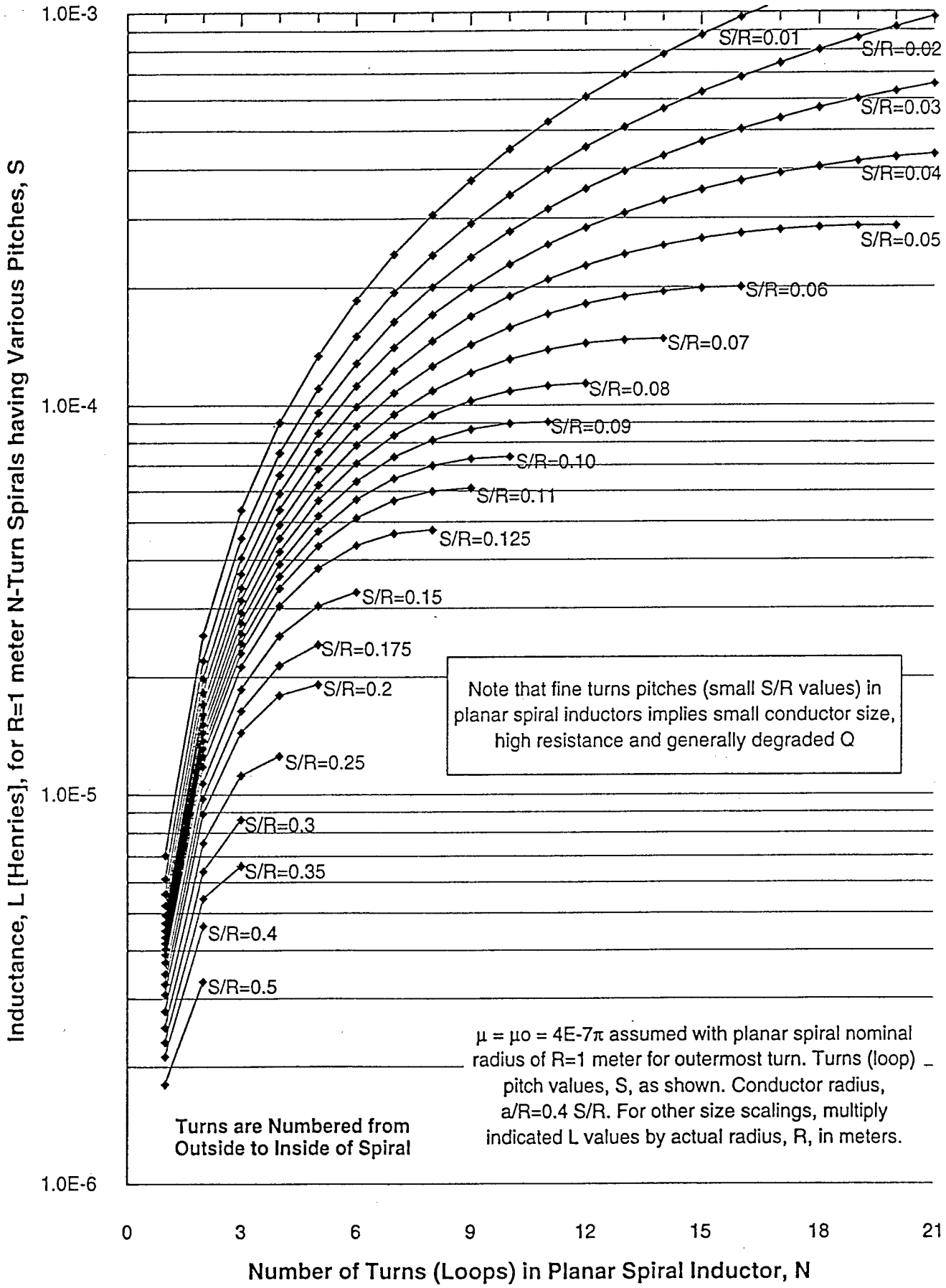

Inductance vs. Number of Turns for R=1 meter Spirals with Various Pitches, S/R
1.0E-3
1.0E-4
1.0E-5
1.0E-6
Inductance, L [Henries], for R=1 meter N-Turn Spirals having Various Pitches, S
S/R=0.01
S/R=0.02
S/R=0.03
S/R=0.04
S/R=0.05
S/R=0.06
S/R=0.07
S/R=0.08
S/R=0.09
S/R=0.10
S/R=0.11
S/R=0.125
S/R=0.15
S/R=0.175
S/R=0.2
S/R=0.25
S/R=0.3
S/R=0.35
S/R=0.4
S/R=0.5
Note that fine turns pitches (small S/R values) in planar spiral inductors implies small conductor size, high resistance and generally degraded Q
μ = μo = 4E-7π assumed with planar spiral nominal radius of R=1 meter for outermost turn. Turns (loop) pitch values, S, as shown. Conductor radius, a/R=0.4 S/R. For other size scalings, multiply indicated L values by actual radius, R, in meters.
Turns are Numbered from Outside to Inside of Spiral
0
3
6
9
12
15
18
21
Number of Turns (Loops) in Planar Spiral Inductor, N

FIGURE 16.

Summary of R=1 meter Spiral Inductor L vs. N Data for Various Turn Pitches, S/R
L Values Include Very Low Frequency Internal Self-Inductance; Conductor Radius a/R=0.4S/R

Richard C. Eden 7/14/96 R is Radius of Center of Conductor of Outer (N=1) Loop; Turns are Numbered from Outside In

S/R=	0.5	0.4	0.35	0.3	0.25	0.2	0.175	0.15	0.125	0.11	0.1
a/R=	0.2	0.16	0.14	0.12	0.1	0.08	0.07	0.06	0.05	0.044	0.04
N=											
1	1.80693E-6	2.12466E-6	2.31401E-6	2.53147E-6	2.78685E-6	3.07932E-6	3.28017E-6	3.49079E-6	3.73797E-6	3.91009E-6	4.03782E-6
2	3.32221E-6	4.63437E-6	5.45178E-6	6.40991E-6	7.54712E-6	8.91154E-6	9.76003E-6	1.06949E-5	1.17808E-5	1.25441E-5	1.31034E-5
3			6.60564E-6	8.61724E-6	1.11706E-5	1.43829E-5	1.63695E-5	1.86234E-5	2.12612E-5	2.30873E-5	2.44387E-5
4					1.25240E-5	1.79452E-5	2.14511E-5	2.55404E-5	3.04004E-5	3.37773E-5	3.62913E-5
5						1.91843E-5	2.42398E-5	3.04553E-5	3.80736E-5	4.34486E-5	4.74862E-5
6								3.29912E-5	4.35911E-5	5.12883E-5	5.71472E-5
7									4.67093E-5	5.68462E-5	6.46991E-5
8									4.77009E-5	6.00085E-5	6.98812E-5
9										6.10858E-5	7.27081E-5
10											7.35823E-5

S/R=	0.1	0.09	0.08	0.07	0.06	0.05	0.04	0.03	0.02	0.01
a/R=	0.04	0.036	0.032	0.028	0.024	0.02	0.016	0.012	0.008	0.004
N=										
1	4.03782E-6	4.17845E-6	4.33498E-6	4.51164E-6	4.71459E-6	4.95338E-6	5.24400E-6	5.61637E-6	6.13762E-6	7.02172E-6
2	1.31034E-5	1.37198E-5	1.44066E-5	1.51037E-5	1.60289E-5	1.70166E-5	1.82782E-5	1.98049E-5	2.20282E-5	2.56446E-5
3	2.44387E-5	2.59378E-5	2.75602E-5	2.93157E-5	3.14594E-5	3.38362E-5	3.67819E-5	4.04602E-5	4.55196E-5	5.37444E-5
4	3.62913E-5	3.90932E-5	4.21170E-5	4.54634E-5	4.93945E-5	5.38687E-5	5.92731E-5	6.60919E-5	7.54208E-5	9.02456E-5
5	4.74862E-5	5.19656E-5	5.68561E-5	6.23576E-5	6.86707E-5	7.59864E-5	8.46940E-5	9.57371E-5	1.10621E-4	1.34366E-4
6	5.71472E-5	6.36728E-5	7.08823E-5	7.89810E-5	8.83543E-5	9.92099E-5	1.12172E-4	1.28403E-4	1.50466E-4	1.85419E-4
7	6.46991E-5	7.35596E-5	8.34714E-5	9.46804E-5	1.07679E-4	1.22773E-4	1.40859E-4	1.63492E-4	1.94161E-4	2.42875E-4
8	6.98812E-5	8.12299E-5	9.41177E-5	1.08857E-4	1.26022E-4	1.46062E-4	1.70162E-4	2.00341E-4	2.41200E-4	3.05878E-4
9	7.27081E-5	8.64947E-5	1.02502E-4	1.21056E-4	1.42865E-4	1.68528E-4	1.99510E-4	2.38462E-4	2.91078E-4	3.74376E-4
10	7.35823E-5	8.94271E-5	1.08467E-4	1.31006E-4	1.57836E-4	1.89726E-4	2.28461E-4	2.77279E-4	3.43340E-4	4.47843E-4
11		9.04215E-5	1.12084E-4	1.38558E-4	1.70664E-4	2.09304E-4	2.56560E-4	3.16358E-4	3.97512E-4	5.25868E-4
12			1.13653E-4	1.43714E-4	1.81151E-4	2.26909E-4	2.83446E-4	3.55396E-4	4.53155E-4	6.07908E-4
13				1.46649E-4	1.89217E-4	2.42345E-4	3.08804E-4	3.93965E-4	5.09995E-4	6.93835E-4
14				1.47757E-4	1.94895E-4	2.55462E-4	3.32379E-4	4.31747E-4	5.67656E-4	7.83331E-4
15					1.98363E-4	2.66162E-4	3.53918E-4	4.68461E-4	6.25831E-4	8.76164E-4
16					1.99953E-4	2.74454E-4	3.73303E-4	5.03867E-4	6.84301E-4	9.72065E-4
17						2.80401E-4	3.90360E-4	5.37700E-4	7.42763E-4	1.07074E-3
18						2.84190E-4	4.05015E-4	5.69790E-4	8.00914E-4	1.17203E-3
19						2.86131E-4	4.17257E-4	5.99944E-4	8.58640E-4	1.27546E-3
20						2.86697E-4	4.27098E-4	6.28028E-4	9.15659E-4	1.38094E-3
21							4.34603E-4	6.53941E-4	9.71786E-4	1.48839E-3

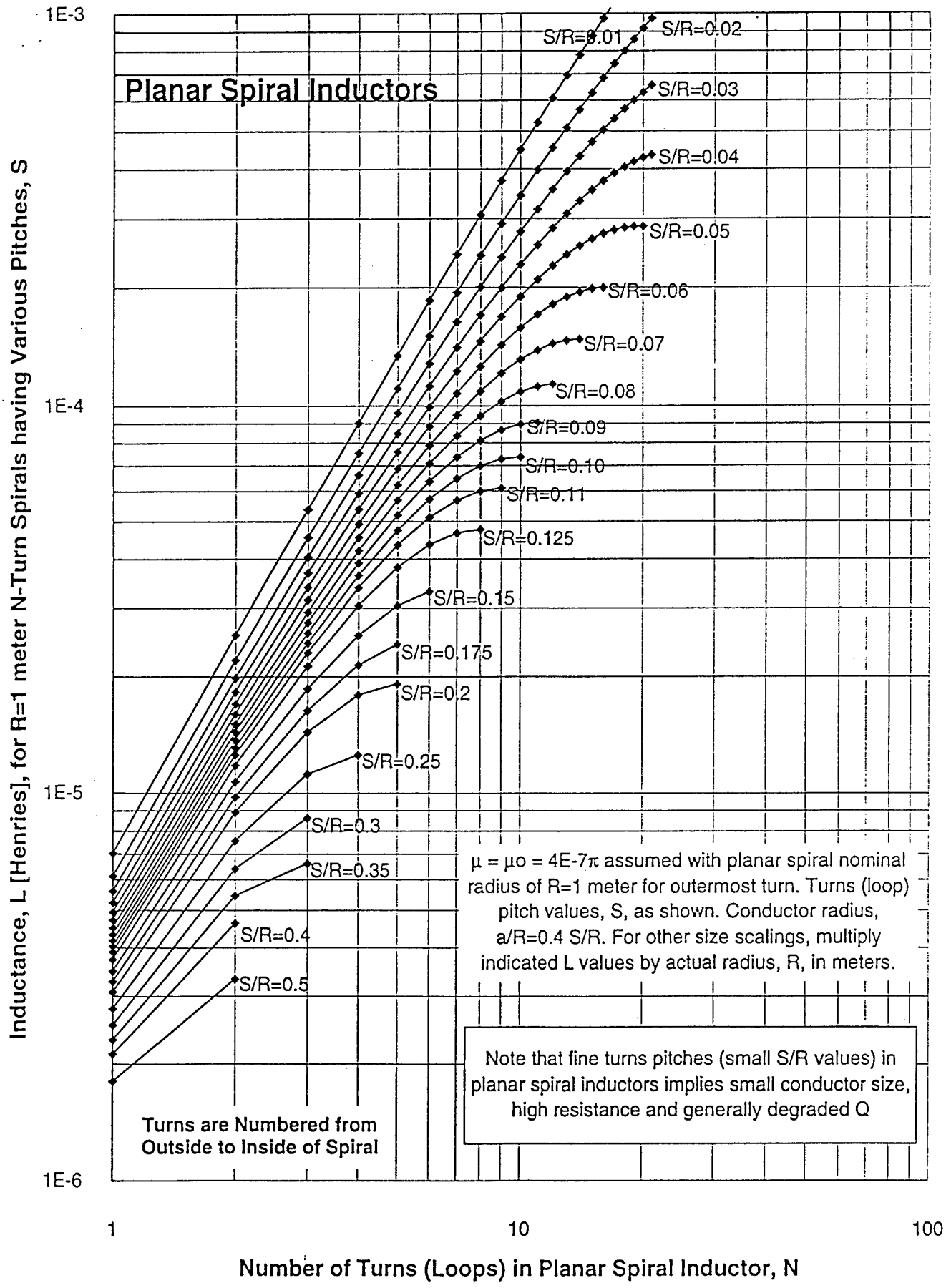

Inductance vs. Number of Turns for R=1 meter Spirals with Various Pitches, S/R
Planar Spiral Inductors
S/R=0.01
S/R=0.02
S/R=0.03
S/R=0.04
S/R=0.05
S/R=0.06
S/R=0.07
S/R=0.08
S/R=0.09
S/R=0.10
S/R=0.11
S/R=0.125
S/R=0.15
S/R=0.175
S/R=0.2
S/R=0.25
S/R=0.3
S/R=0.35
S/R=0.4
S/R=0.5
μ = μo = 4E-7π assumed with planar spiral nominal radius of R=1 meter for outermost turn. Turns (loop) pitch values, S, as shown. Conductor radius, a/R=0.4 S/R. For other size scalings, multiply indicated L values by actual radius, R, in meters.
Note that fine turns pitches (small S/R values) in planar spiral inductors implies small conductor size, high resistance and generally degraded Q
Turns are Numbered from Outside to Inside of Spiral
1E-3
1E-4
1E-5
1E-6
Inductance, L [Henries], for R=1 meter N-Turn Spirals having Various Pitches, S
1
10
100
Number of Turns (Loops) in Planar Spiral Inductor, N

FIGURE 17.

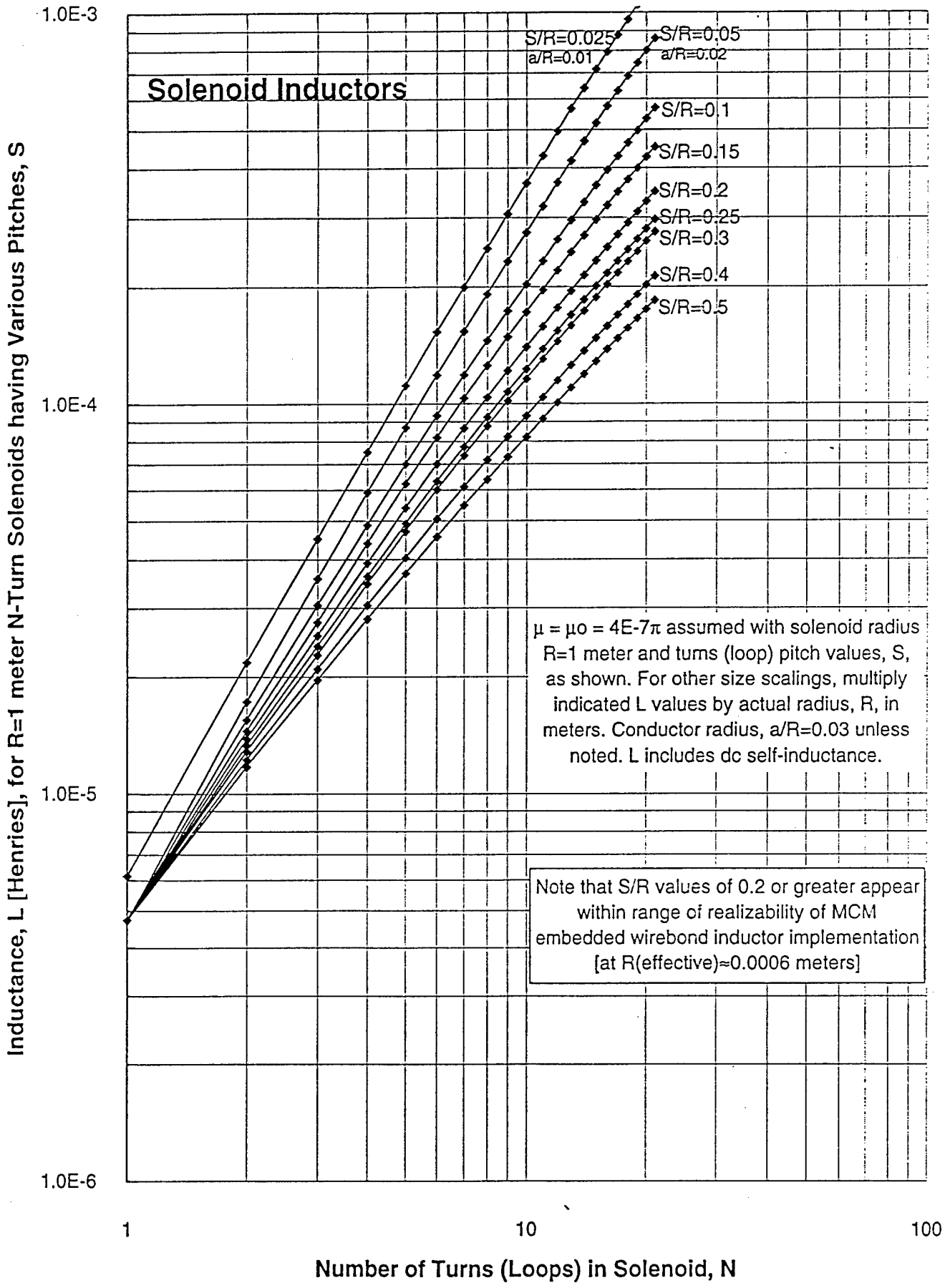
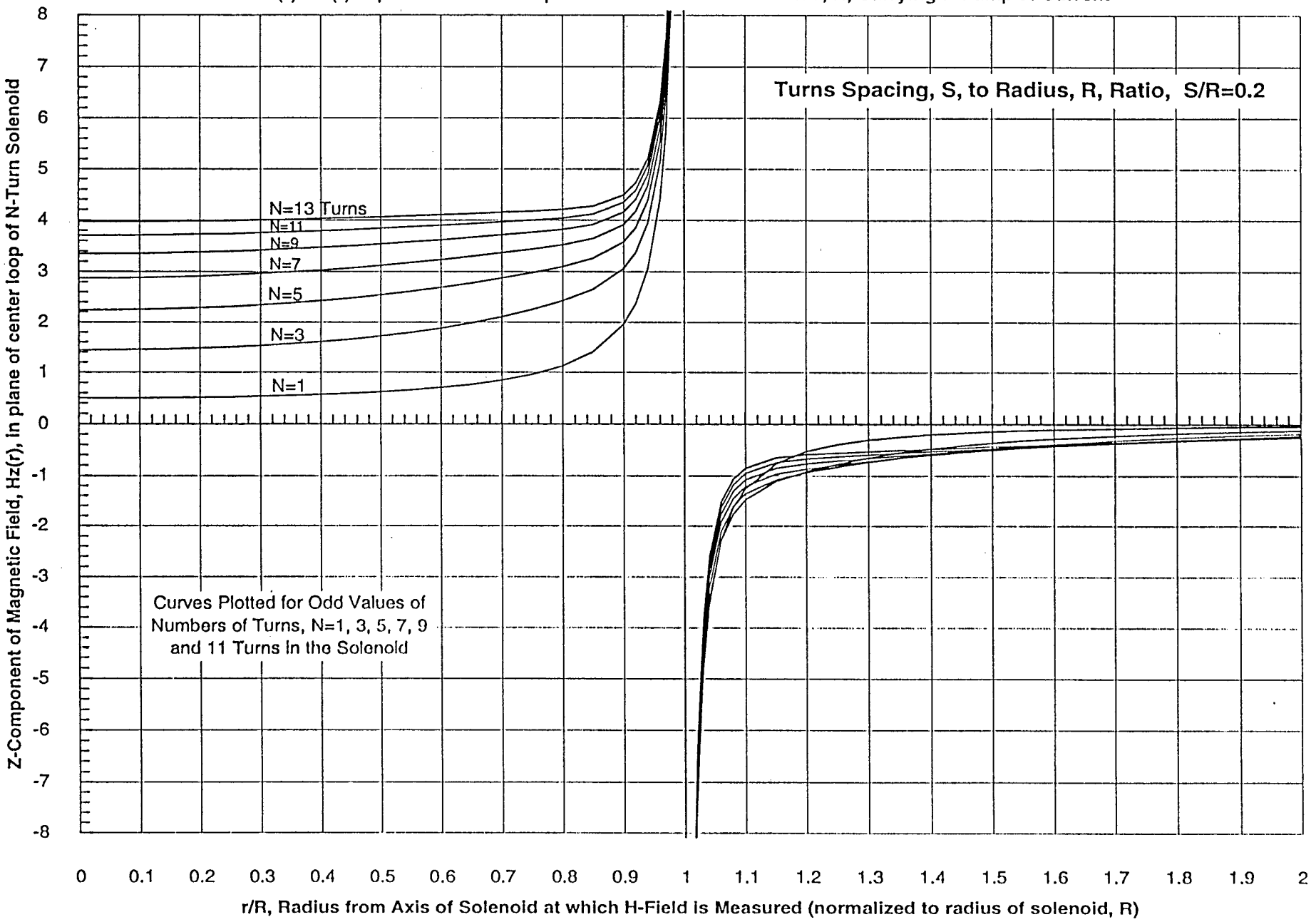

Inductance vs. Number of Turns for R=1 meter Solenoids with Various Pitches, S/R
Solenoid Inductors
S/R=0.025
a/R=0.01
S/R=0.05
a/R=0.02
S/R=0.1
S/R=0.15
S/R=0.2
S/R=0.25
S/R=0.3
S/R=0.4
S/R=0.5
μ = μo = 4E-7π assumed with solenoid radius R=1 meter and turns (loop) pitch values, S, as shown. For other size scalings, multiply indicated L values by actual radius, R, in meters. Conductor radius, a/R=0.03 unless noted. L includes dc self-inductance.
Note that S/R values of 0.2 or greater appear within range of realizability of MCM embedded wirebond inductor implementation [at R(effective)≈0.0006 meters]
Inductance, L [Henries], for R=1 meter N-Turn Solenoids having Various Pitches, S
1.0E-3
1.0E-4
1.0E-5
1.0E-6
1
10
100
Number of Turns (Loops) in Solenoid, N

FIGURE 15.

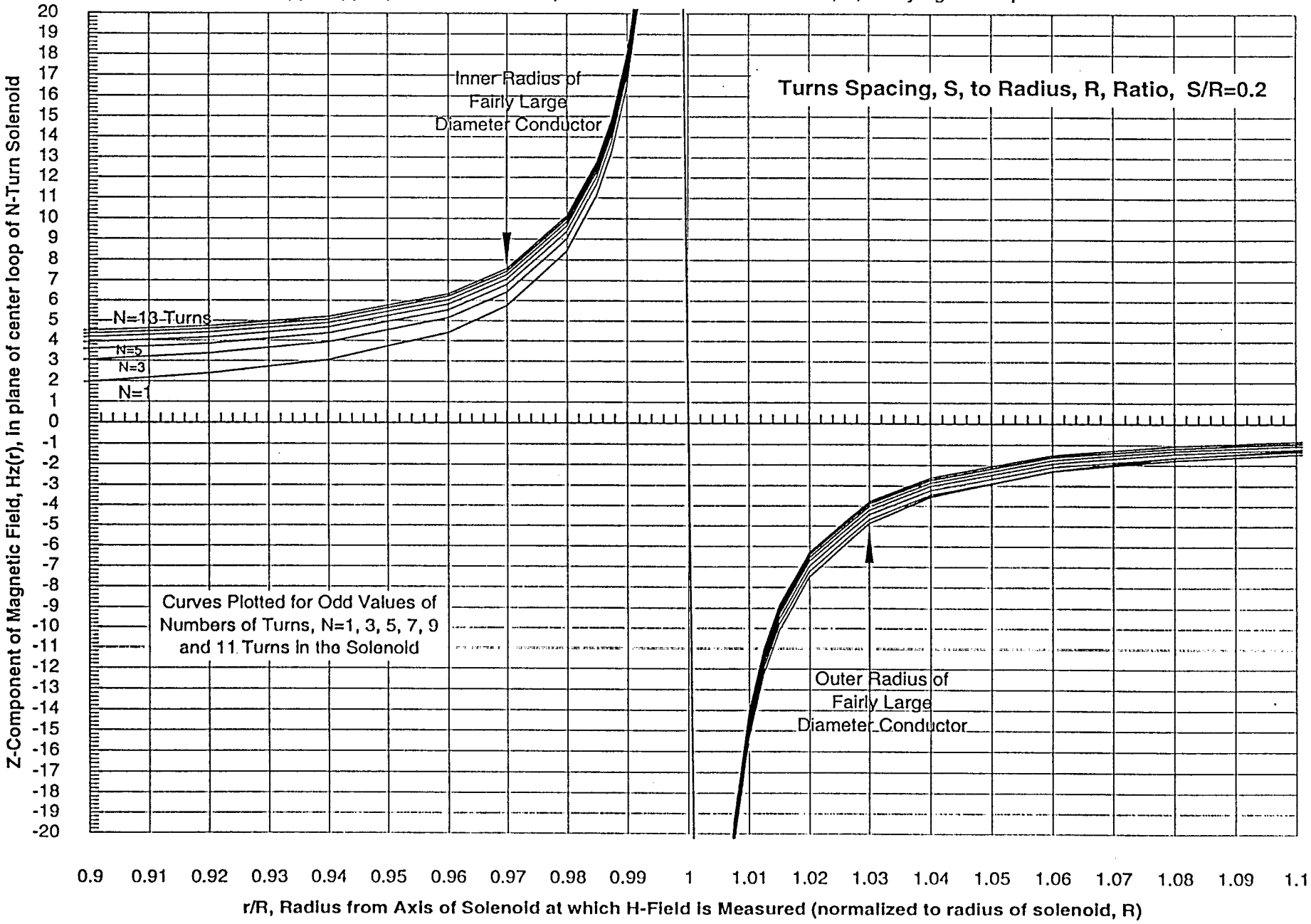
Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.2

H(r)=Hz(r) In plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current



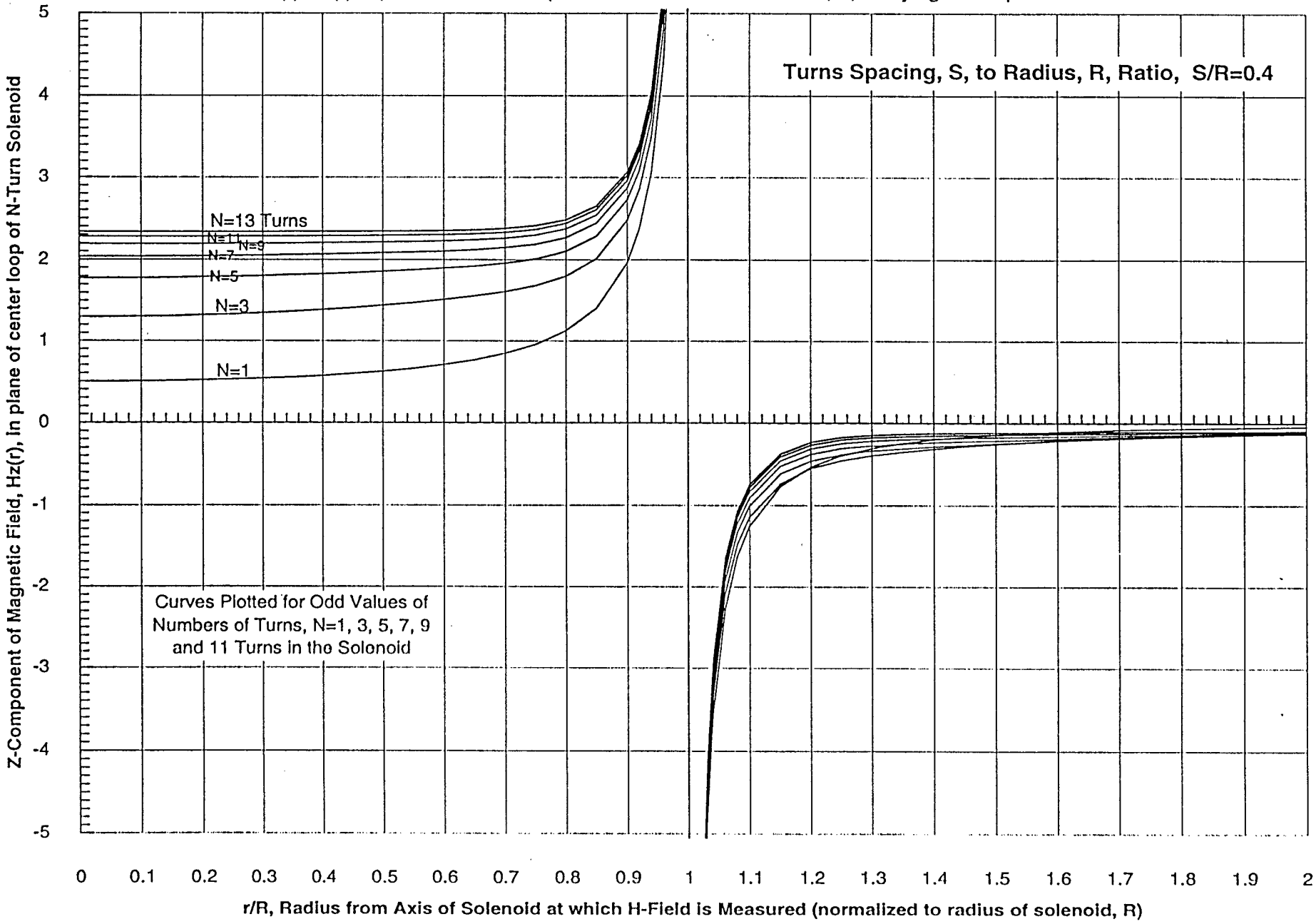
Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.2

H(r)=Hz(r) In plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current



Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.4

H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current



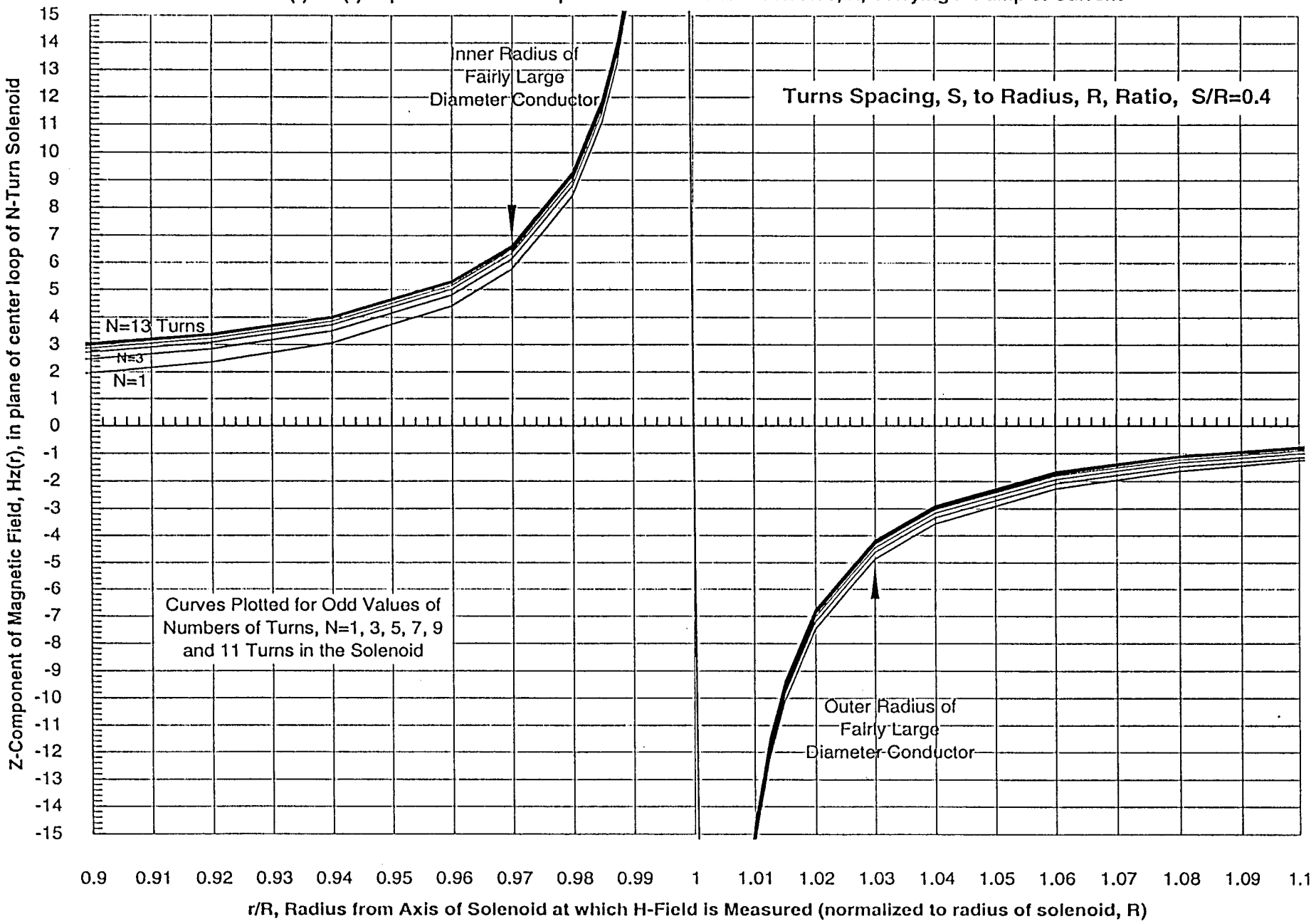

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.4
H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current
Z-Component of Magnetic Field, Hz(r), in plane of center loop of N-Turn Solenoid
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
-15
Inner Radius of Fairly Large Diameter Conductor
Turns Spacing, S, to Radius, R, Ratio, S/R=0.4
N=13 Turns
N=3
N=1
Curves Plotted for Odd Values of Numbers of Turns, N=1, 3, 5, 7, 9 and 11 Turns in the Solenoid
Outer Radius of Fairly Large Diameter Conductor
0.9
0.91
0.92
0.93
0.94
0.95
0.96
0.97
0.98
0.99
1
1.01
1.02
1.03
1.04
1.05
1.06
1.07
1.08
1.09
1.1
r/R, Radius from Axis of Solenoid at which H-Field is Measured (normalized to radius of solenoid, R)

FIGURE 21.

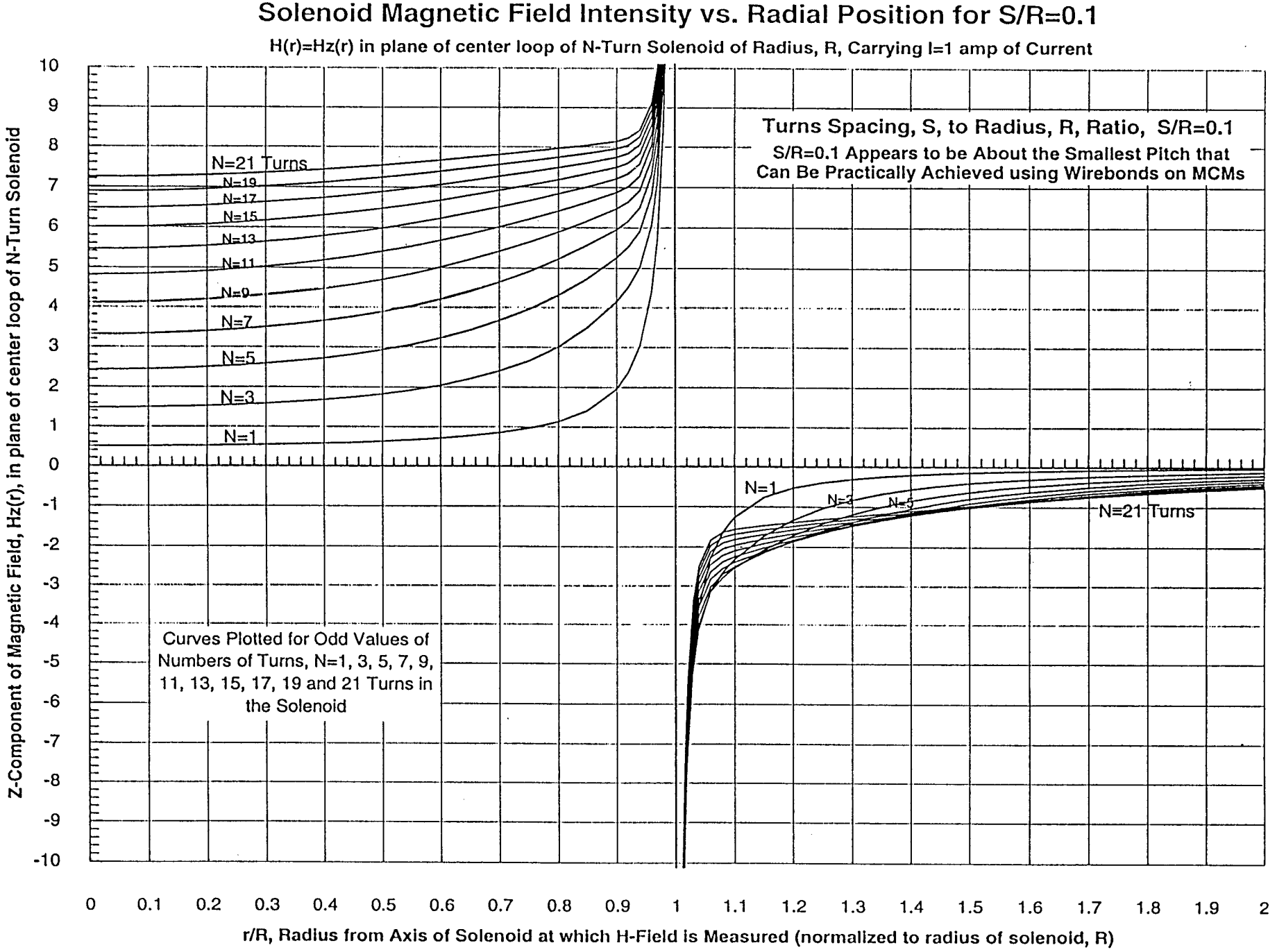

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.1
H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current
Turns Spacing, S, to Radius, R, Ratio, S/R=0.1
S/R=0.1 Appears to be About the Smallest Pitch that Can Be Practically Achieved using Wirebonds on MCMs
N=21 Turns
N=19
N=17
N=15
N=13
N=11
N=9
N=7
N=5
N=3
N=1
N=1
N=3
N=5
N=21 Turns
Curves Plotted for Odd Values of Numbers of Turns, N=1, 3, 5, 7, 9, 11, 13, 15, 17, 19 and 21 Turns in the Solenoid
Z-Component of Magnetic Field, Hz(r), in plane of center loop of N-Turn Solenoid
10
9
8
7
6
5
4
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
1.9
2
r/R, Radius from Axis of Solenoid at which H-Field is Measured (normalized to radius of solenoid, R)

FIGURE 21a

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.1

H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current

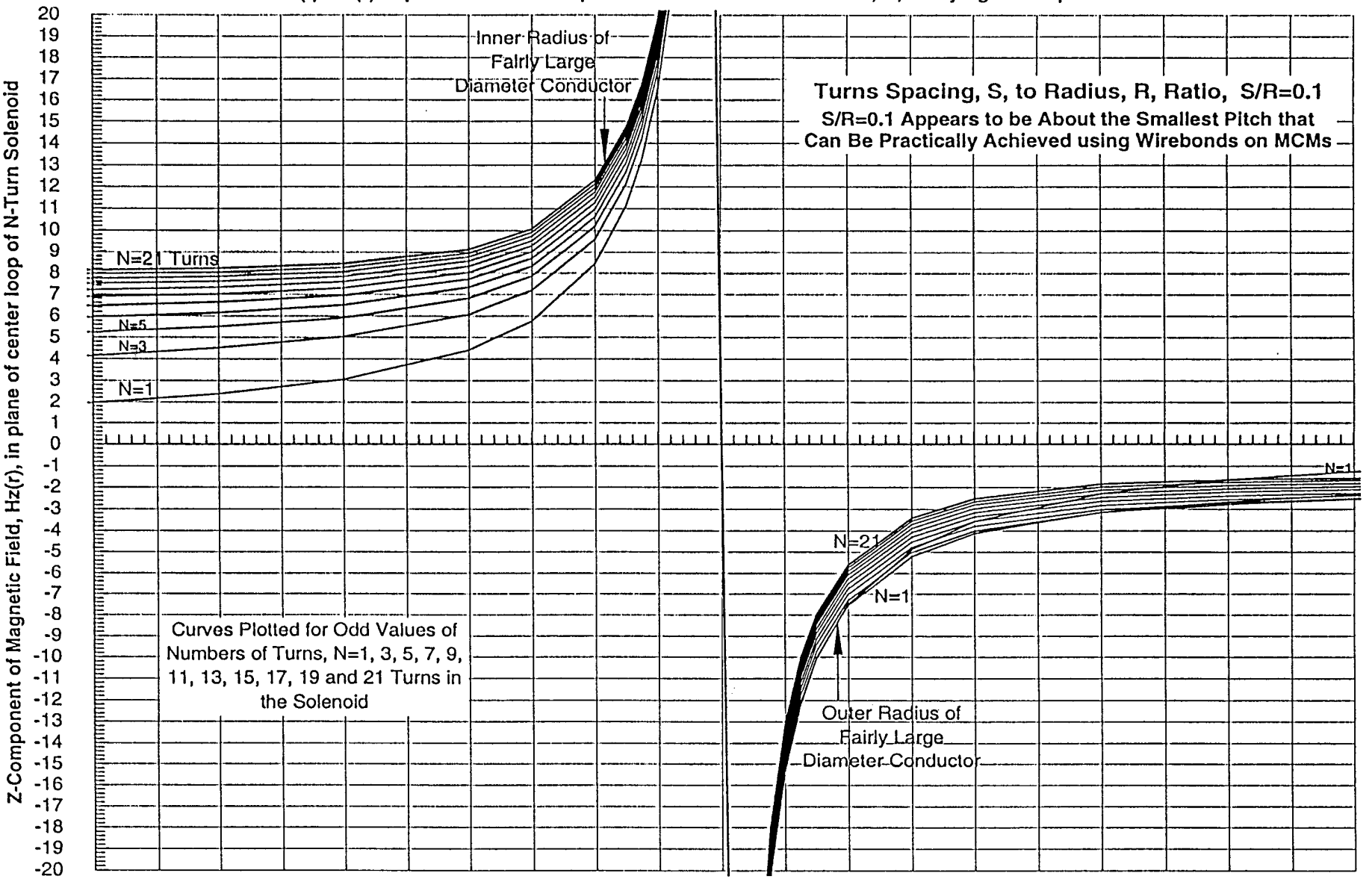


Figure 21b.

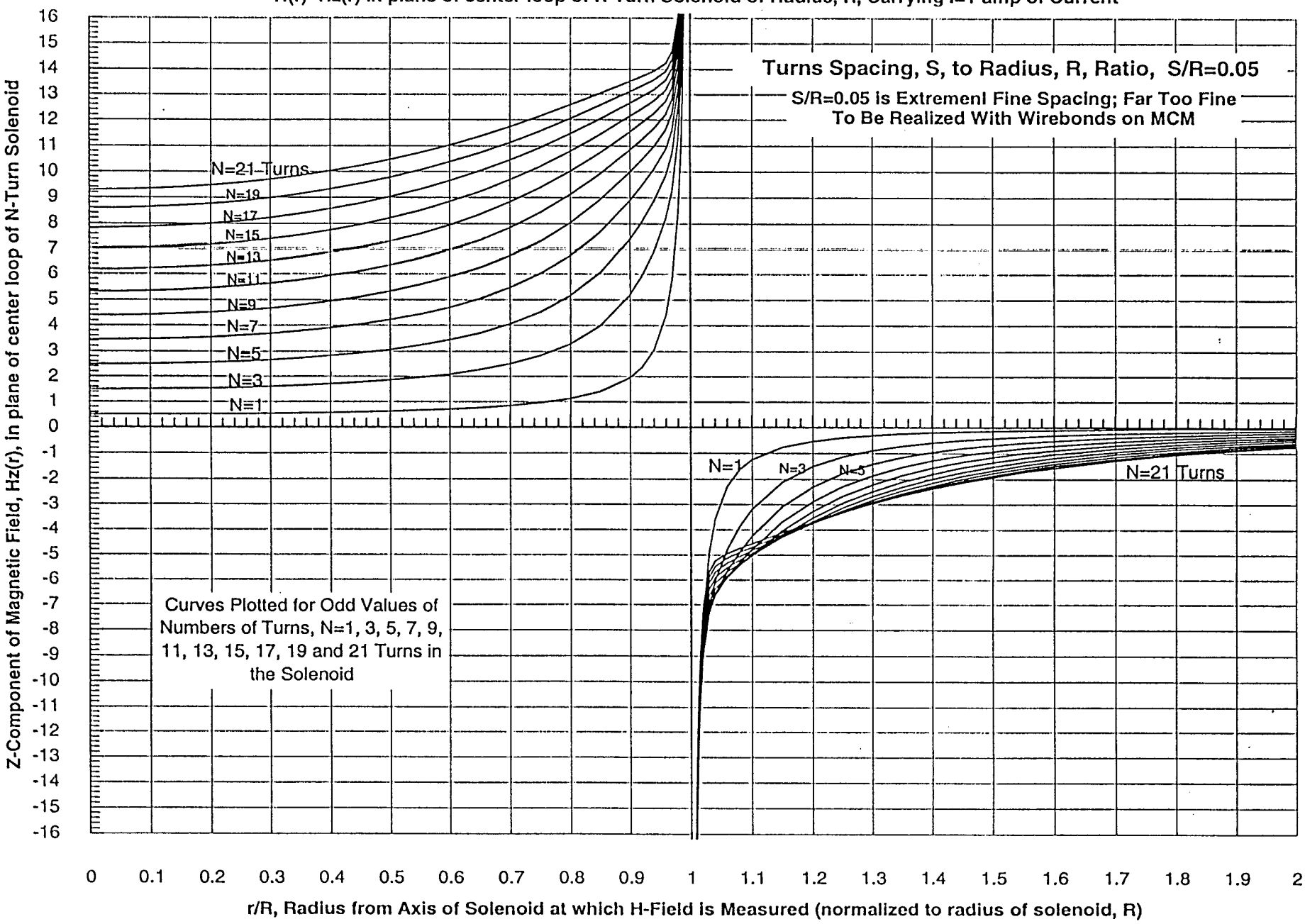

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.05
H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current
Turns Spacing, S, to Radius, R, Ratio, S/R=0.05
S/R=0.05 is Extremenl Fine Spacing; Far Too Fine To Be Realized With Wirebonds on MCM
N=21 Turns
N=19
N=17
N=15
N=13
N=11
N=9
N=7
N=5
N=3
N=1
N=1
N=3
N=5
N=21 Turns
Curves Plotted for Odd Values of Numbers of Turns, N=1, 3, 5, 7, 9, 11, 13, 15, 17, 19 and 21 Turns in the Solenoid
Z-Component of Magnetic Field, Hz(r), in plane of center loop of N-Turn Solenoid
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14 -15 -16
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2
r/R, Radius from Axis of Solenoid at which H-Field is Measured (normalized to radius of solenoid, R)

FIGURE 22a.

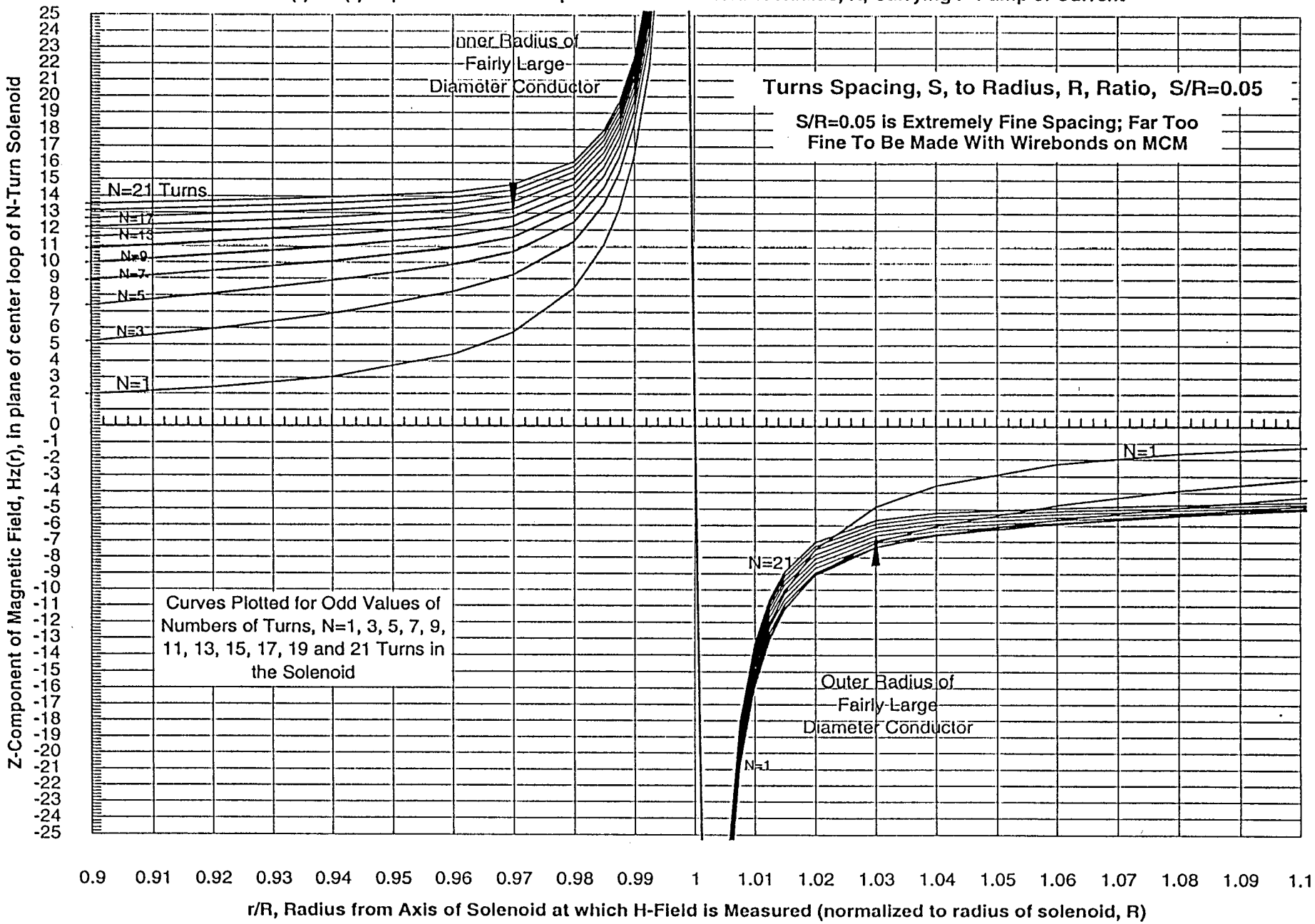

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.05
H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current
Z-Component of Magnetic Field, Hz(r), in plane of center loop of N-Turn Solenoid
Inner Radius of
-Fairly Large-
Diameter Conductor
Turns Spacing, S, to Radius, R, Ratio, S/R=0.05
S/R=0.05 is Extremely Fine Spacing; Far Too
Fine To Be Made With Wirebonds on MCM
N=21 Turns
N=17
N=13
N=9
N=7
N=5
N=3
N=1
N=1
N=21
Curves Plotted for Odd Values of
Numbers of Turns, N=1, 3, 5, 7, 9,
11, 13, 15, 17, 19 and 21 Turns in
the Solenoid
Outer Radius of
-Fairly Large-
Diameter Conductor
N=1
25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14 -15 -16 -17 -18 -19 -20 -21 -22 -23 -24 -25
0.9 0.91 0.92 0.93 0.94 0.95 0.96 0.97 0.98 0.99 1 1.01 1.02 1.03 1.04 1.05 1.06 1.07 1.08 1.09 1.1
r/R, Radius from Axis of Solenoid at which H-Field is Measured (normalized to radius of solenoid, R)

FIGURE 22b.

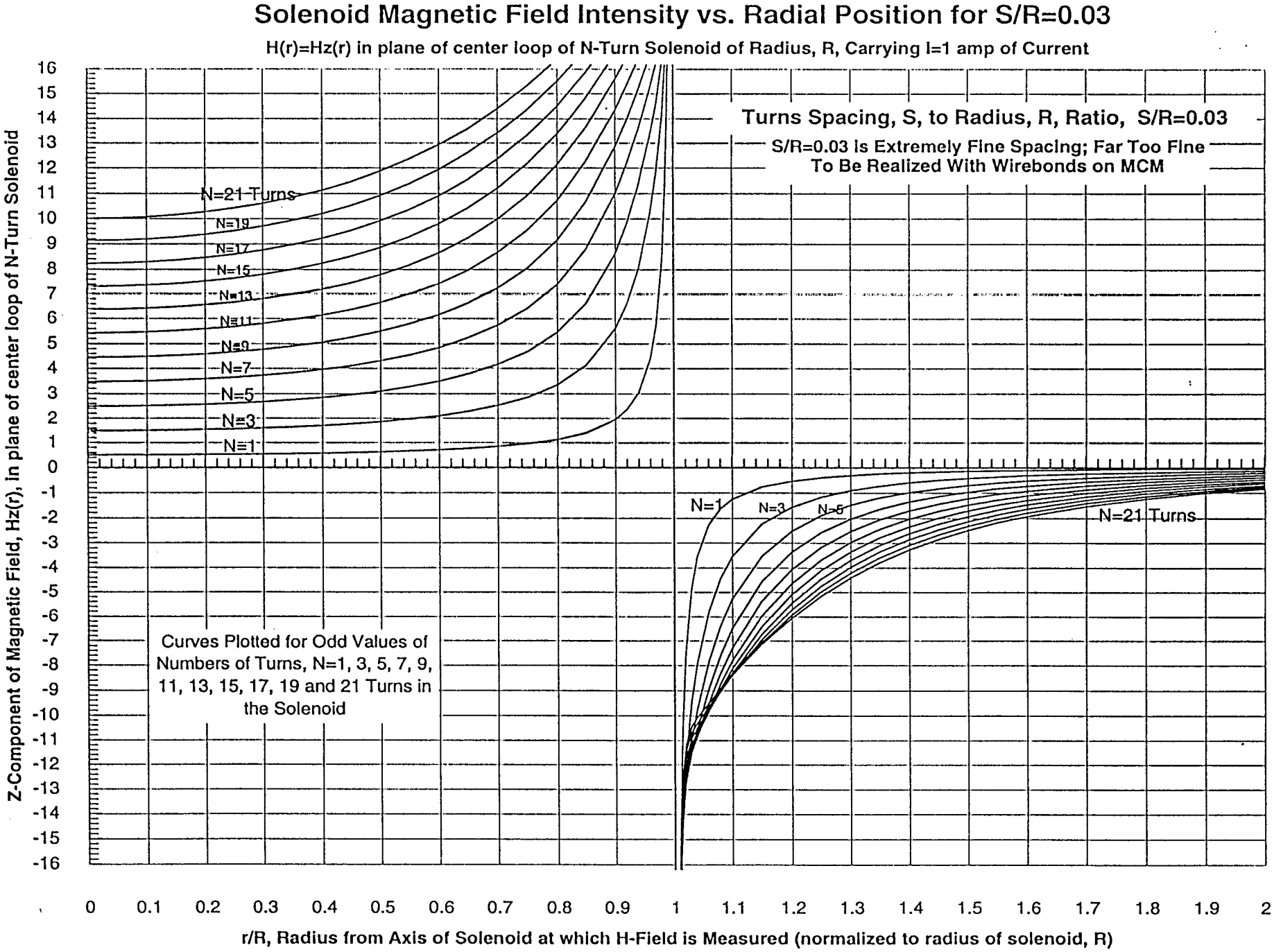

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.03
H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current
Turns Spacing, S, to Radius, R, Ratio, S/R=0.03
S/R=0.03 Is Extremely Fine Spacing; Far Too Fine To Be Realized With Wirebonds on MCM
N=21 Turns
N=19
N=17
N=15
N=13
N=11
N=9
N=7
N=5
N=3
N=1
N=1
N=3
N=5
N=21 Turns
Curves Plotted for Odd Values of Numbers of Turns, N=1, 3, 5, 7, 9, 11, 13, 15, 17, 19 and 21 Turns in the Solenoid
Z-Component of Magnetic Field, Hz(r), in plane of center loop of N-Turn Solenoid
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 -1 -2 -3 -4 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14 -15 -16
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2
r/R, Radius from Axis of Solenoid at which H-Field is Measured (normalized to radius of solenoid, R)

FIGURE 23a.

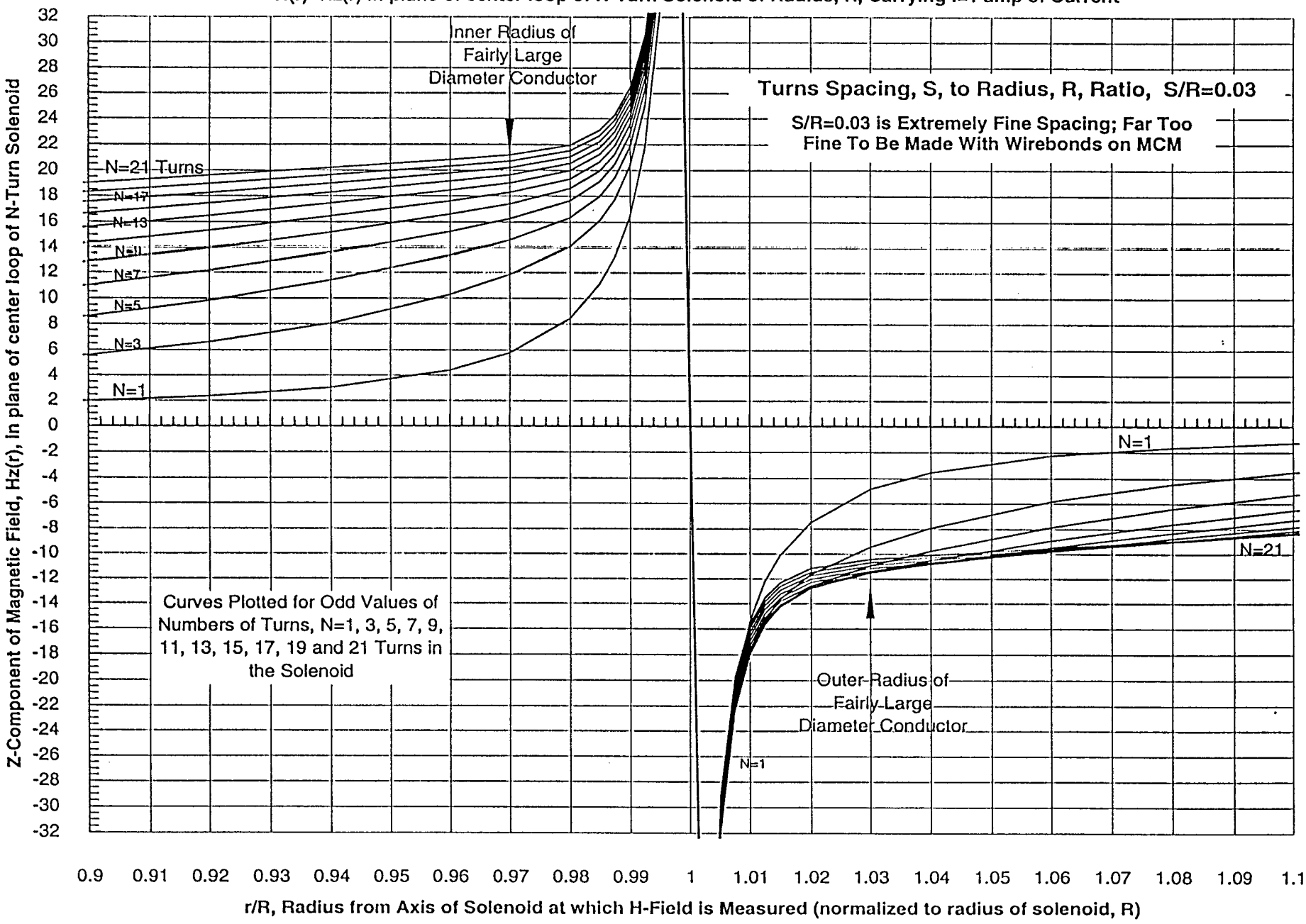

Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.03
H(r)=Hz(r) in plane of center loop of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current
Z-Component of Magnetic Field, Hz(r), in plane of center loop of N-Turn Solenoid
r/R, Radius from Axis of Solenoid at which H-Field is Measured (normalized to radius of solenoid, R)
Inner Radius of Fairly Large Diameter Conductor
Turns Spacing, S, to Radius, R, Ratio, S/R=0.03
S/R=0.03 is Extremely Fine Spacing; Far Too Fine To Be Made With Wirebonds on MCM
N=21 Turns
N=17
N=13
N=11
N=7
N=5
N=3
N=1
Curves Plotted for Odd Values of Numbers of Turns, N=1, 3, 5, 7, 9, 11, 13, 15, 17, 19 and 21 Turns in the Solenoid
Outer Radius of Fairly Large Diameter Conductor
N=1
N=21
32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2 0 -2 -4 -6 -8 -10 -12 -14 -16 -18 -20 -22 -24 -26 -28 -30 -32
0.9 0.91 0.92 0.93 0.94 0.95 0.96 0.97 0.98 0.99 1 1.01 1.02 1.03 1.04 1.05 1.06 1.07 1.08 1.09 1.1

FIGURE 23b.

Definition of Geometry for Ribbon Solenoid Magnetic Field Calculation

Ribbon solenoid is treated as a stack of stacks of parallel circular loops (rather than as a helix). Each ribbon is simulated by 5 closely-spaced (0.03 R stacking pitch) loops, with an implied wire radius of a=0.015R, to simulate a ribbon 0.15R wide x 0.03R thick. The Ribbon stacking pitch is 0.21R, so the nominal gap between turns is 0.06R. H-field is obtained as superposition of H-field of individual circular loops. Highest field will be in plane of center loop, and in that plane, H_r=0 if it is a plane of symmetry.

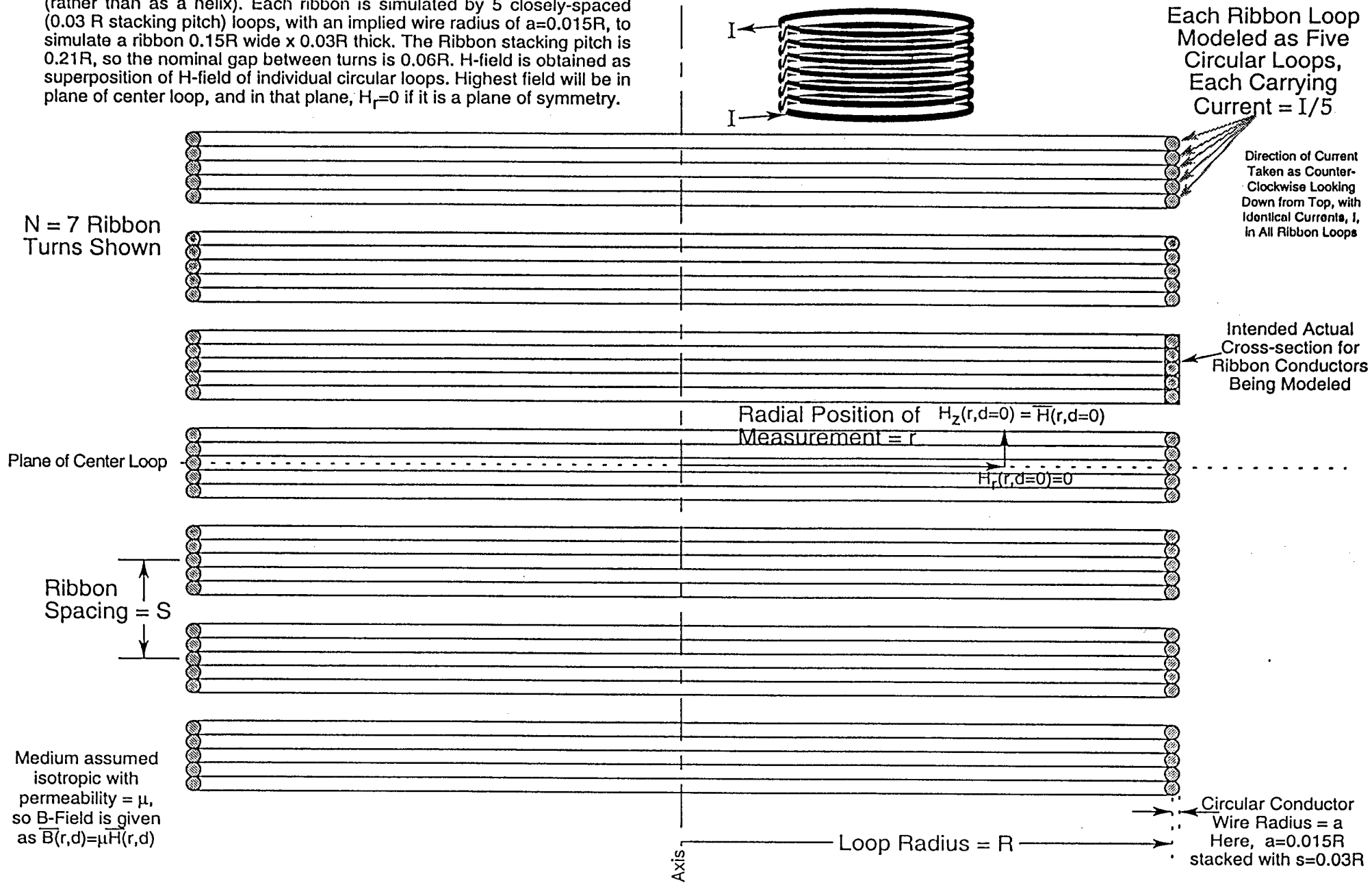


FIGURE 24

0.15Rx0.03R Ribbon Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.21

H(r)=Hz(r) in plane of center 0.15R x 0.03R ribbon conductor of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current

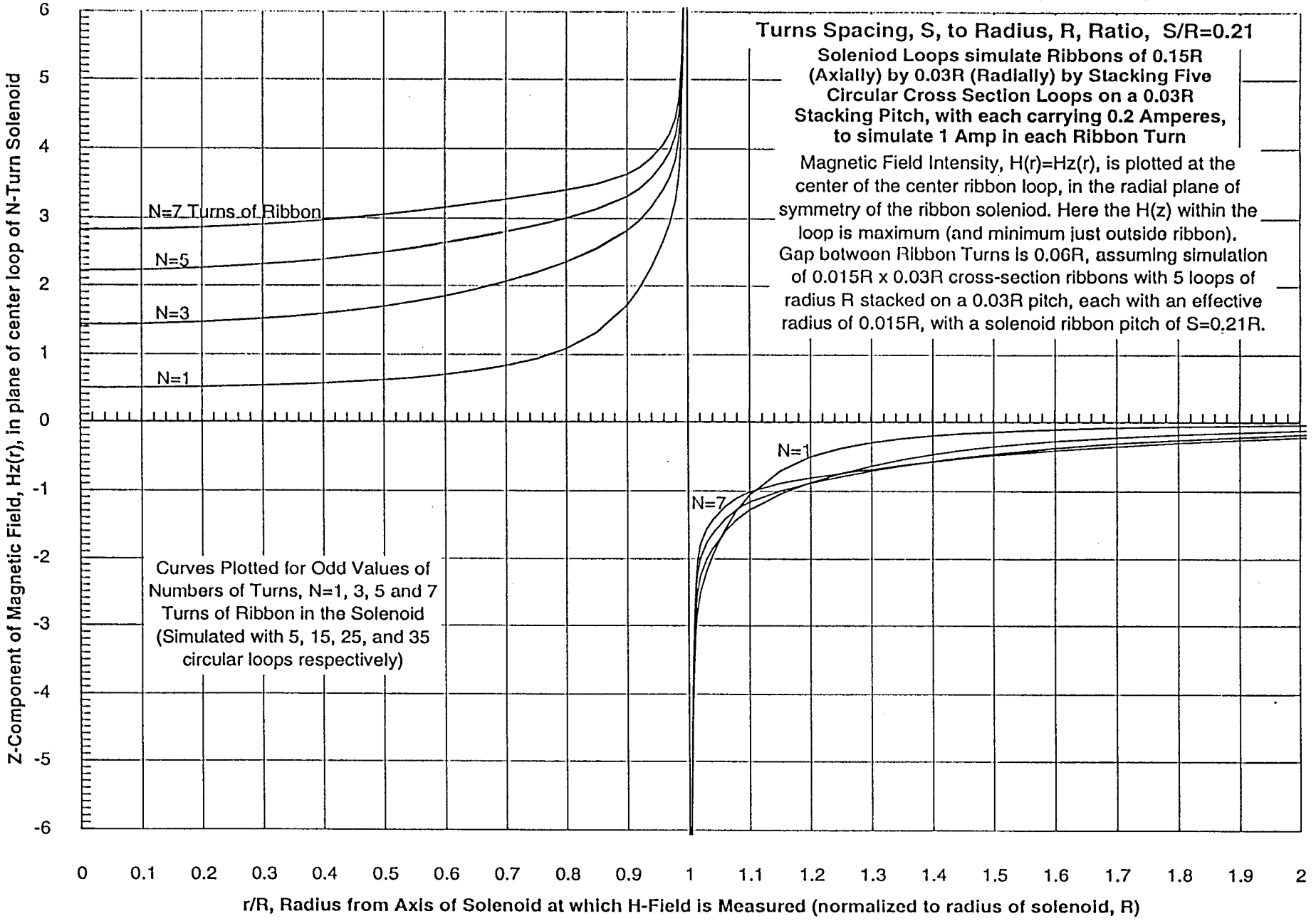


FIGURE 25a.

0.15Rx0.03R Ribbon Solenoid Magnetic Field Intensity vs. Radial Position for S/R=0.21

H(r)=Hz(r) in plane of center 0.15R x 0.03R ribbon conductor of N-Turn Solenoid of Radius, R, Carrying I=1 amp of Current

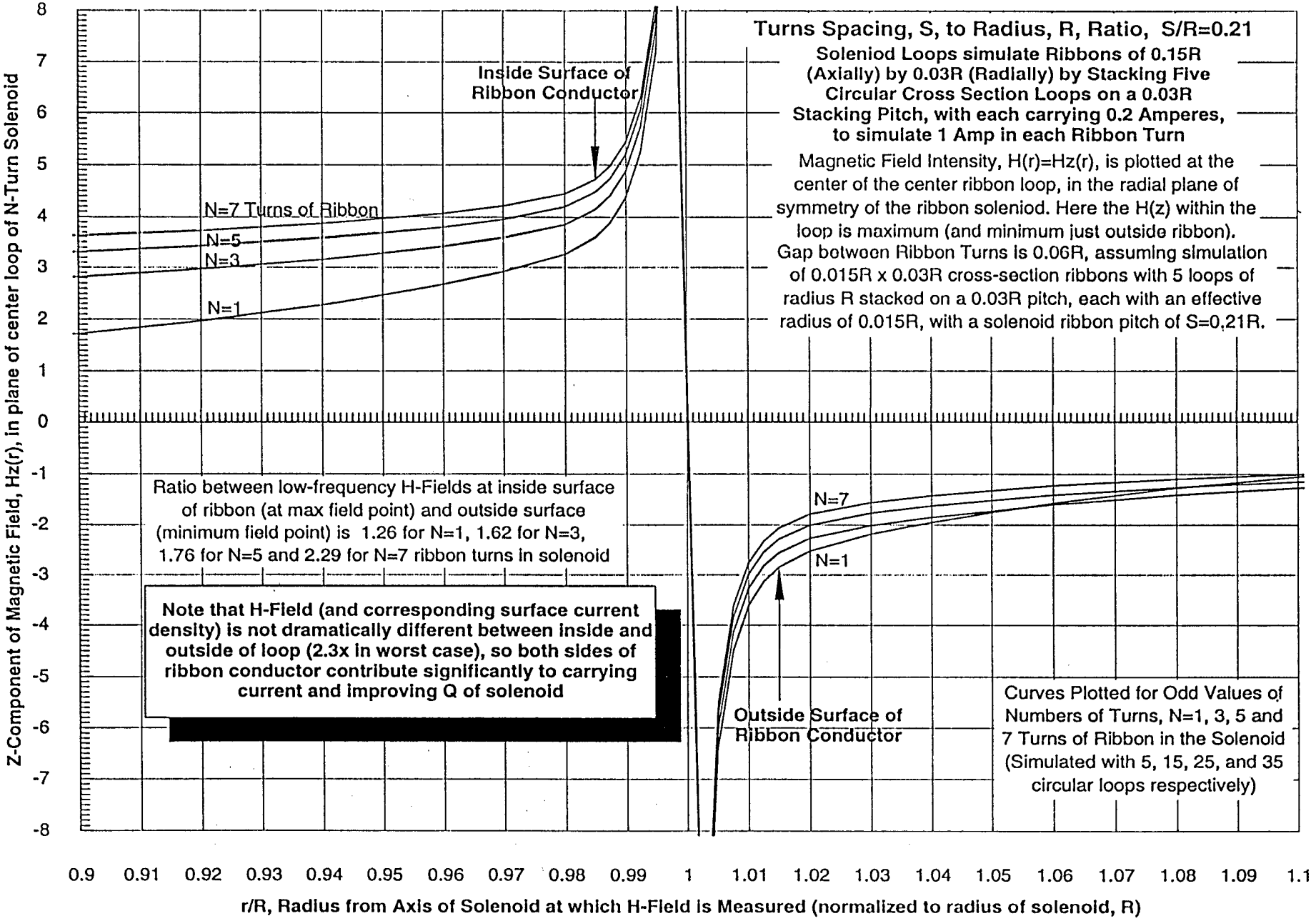


FIGURE 25b

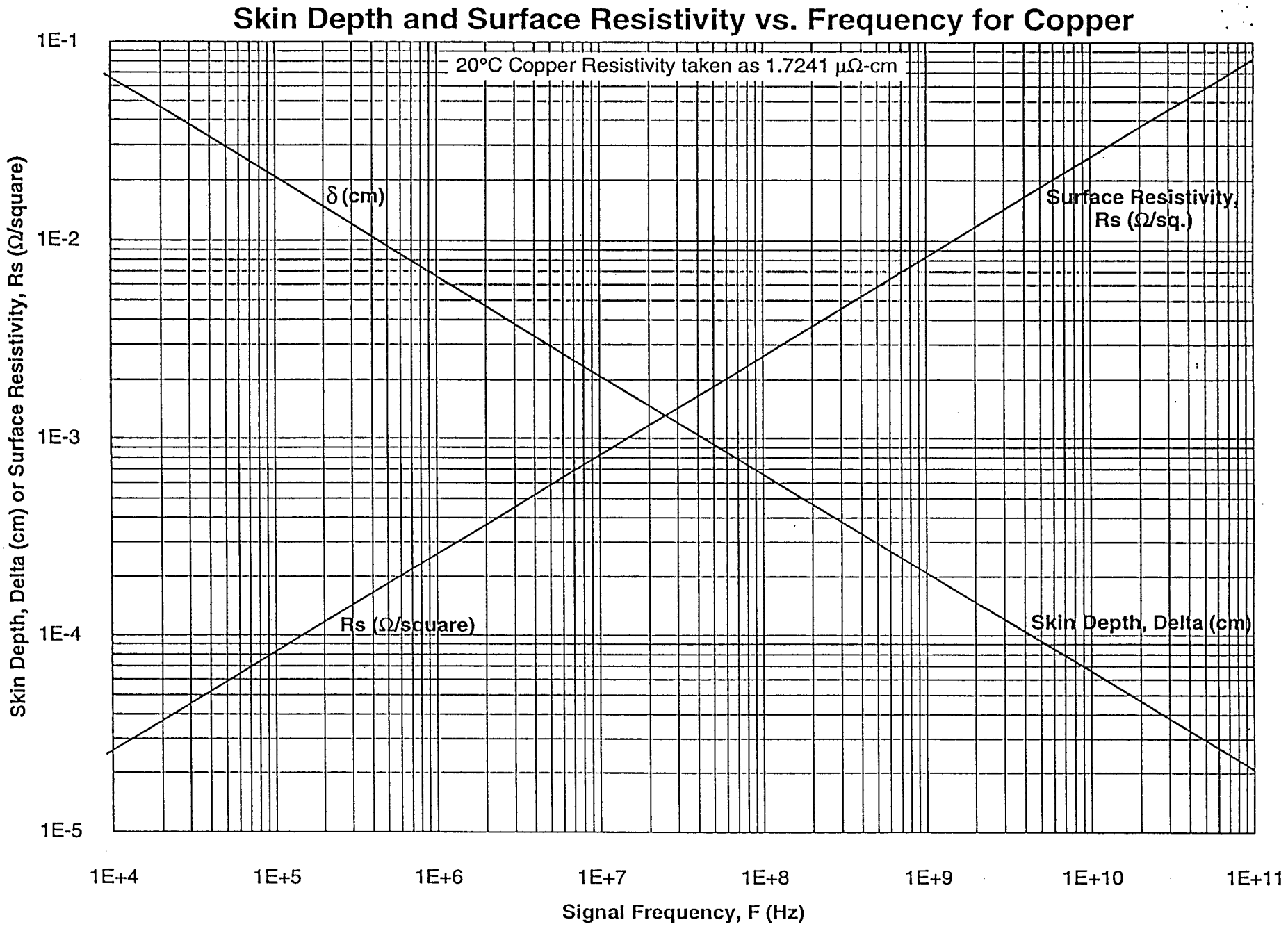

Skin Depth and Surface Resistivity vs. Frequency for Copper
20°C Copper Resistivity taken as 1.7241 μΩ-cm
δ (cm)
Surface Resistivity, Rs (Ω/sq.)
Rs (Ω/square)
Skin Depth, Delta (cm)
Skin Depth, Delta (cm) or Surface Resistivity, Rs (Ω/square)
1E-1
1E-2
1E-3
1E-4
1E-5
1E+4
1E+5
1E+6
1E+7
1E+8
1E+9
1E+10
1E+11
Signal Frequency, F (Hz)

FIGURE 26.

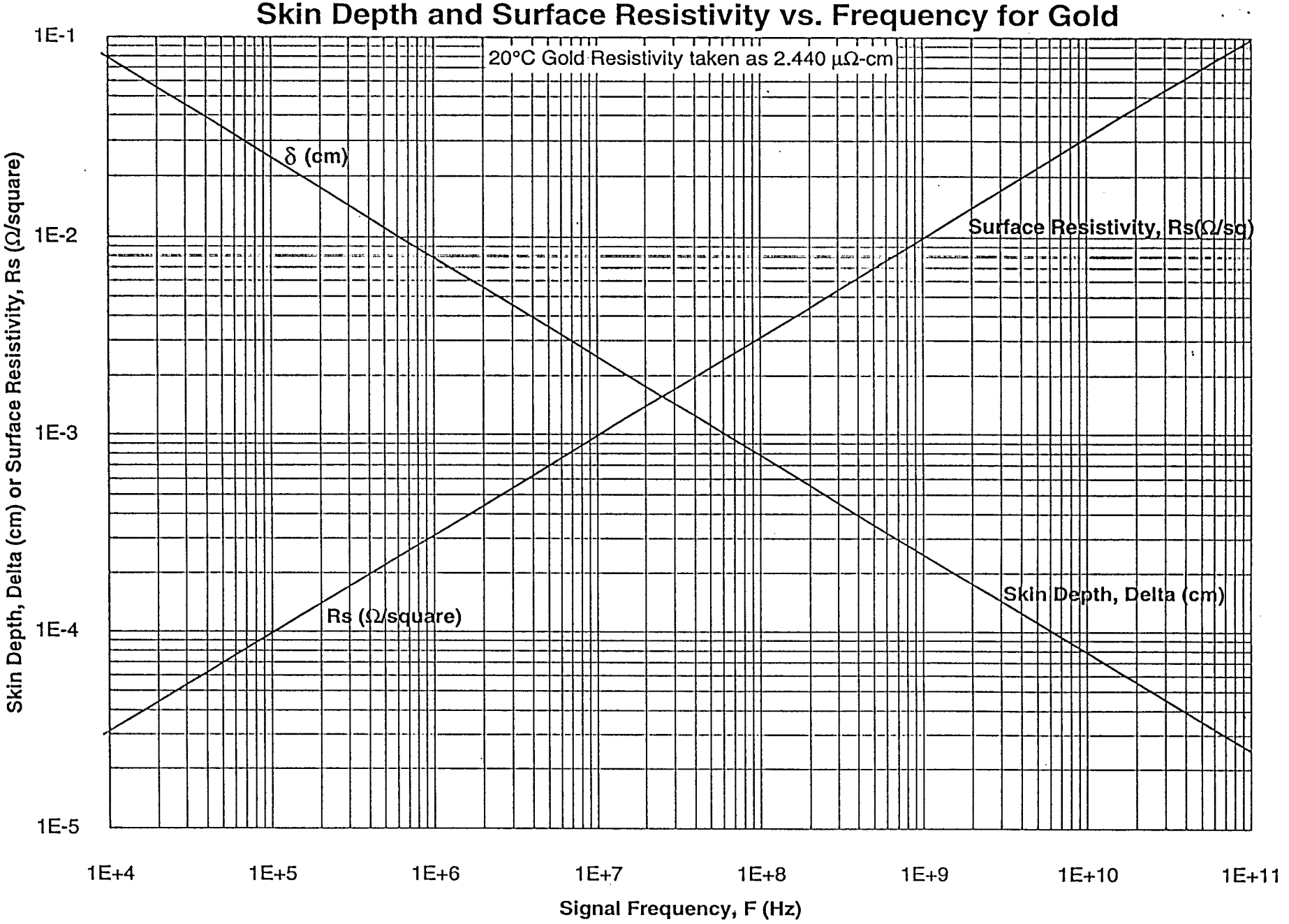
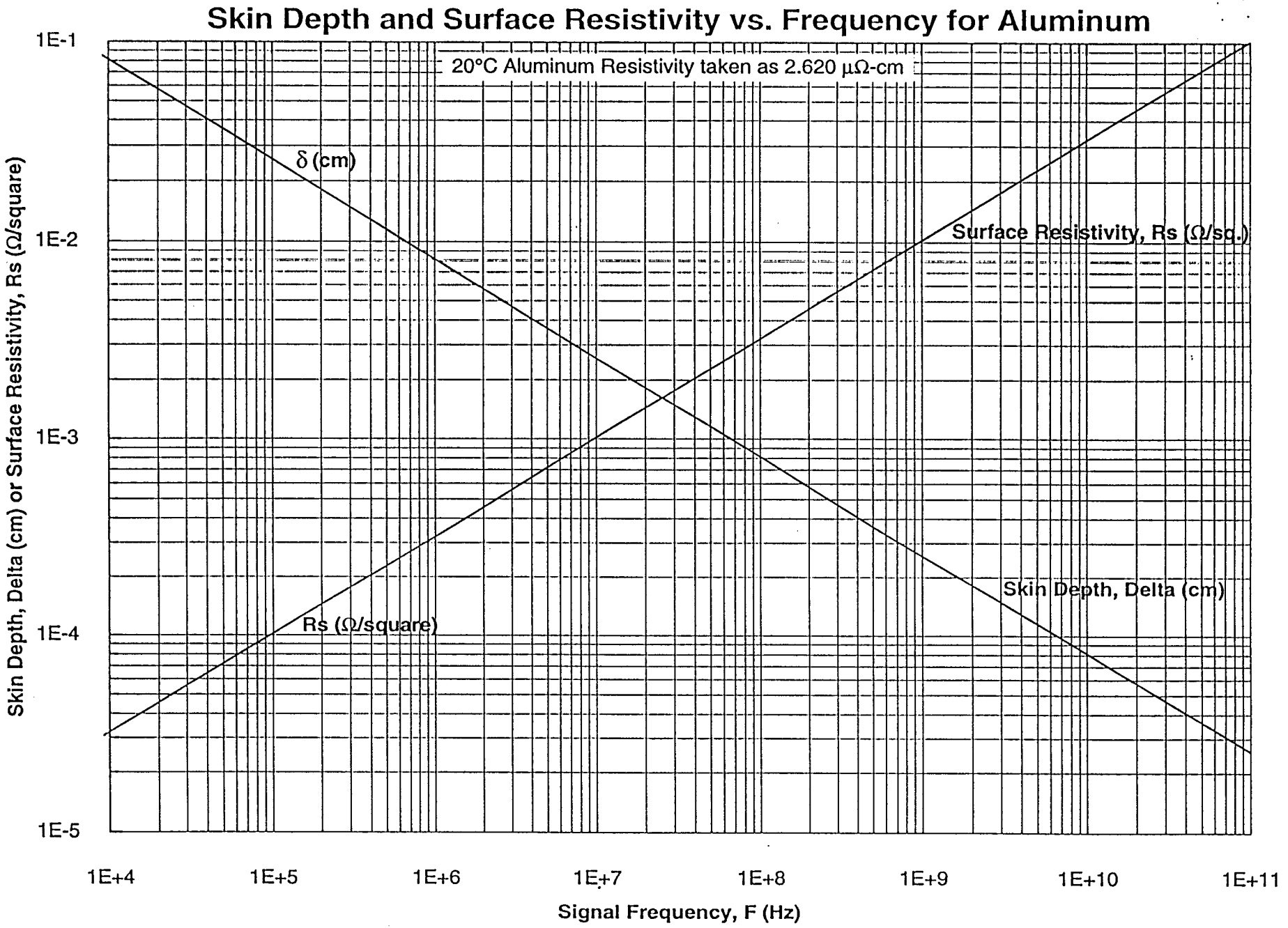

Skin Depth and Surface Resistivity vs. Frequency for Gold
20°C Gold Resistivity taken as 2.440 μΩ-cm
δ (cm)
Surface Resistivity, Rs(Ω/sq)
Rs (Ω/square)
Skin Depth, Delta (cm)
Skin Depth, Delta (cm) or Surface Resistivity, Rs (Ω/square)
1E-1
1E-2
1E-3
1E-4
1E-5
1E+4
1E+5
1E+6
1E+7
1E+8
1E+9
1E+10
1E+11
Signal Frequency, F (Hz)

FIGURE 27


Skin Depth and Surface Resistivity vs. Frequency for Aluminum
20°C Aluminum Resistivity taken as 2.620 μΩ-cm
δ (cm)
Surface Resistivity, Rs (Ω/sq.)
Skin Depth, Delta (cm)
Rs (Ω/square)
1E-1
1E-2
1E-3
1E-4
1E-5
Skin Depth, Delta (cm) or Surface Resistivity, Rs (Ω/square)
1E+4
1E+5
1E+6
1E+7
1E+8
1E+9
1E+10
1E+11
Signal Frequency, F (Hz)

```
// AlRoundWireRsLint_1p5mil  1.5 mil Aluminum Round Wire  R.C.Eden 8/16/96
project x, FRLArr, RsArr, LintArr, j, Zo, mu, C, Rsij, Lext, Lint, R, Z2, Z1oc, freq, Er;
project  Ra, Ro, gam, ZoDC, clt, Eo, ceff, Rs, Ldc, LINTdc, RCENTdc, Rdc;
local i, y, SqtEr, Rsel, w, Sqrtw, zzz, V2t;
// Calculational Parameters
FreqStep=0.25E8;        /* FreqStep for calculation*/
NS=101;              /* Number of frequency steps in calculation */
Inf=1e14;
// Physical Constants: All units are meters, seconds, ohms, farads, henrys, Hertz, etc.
pi=3.14159265358979323846;
j=(0,1);
rSqrt2=1/sqrt(2);
mu=(4E-7)*pi;
clt=2.99792458E8;           /* Speed of Light in m/s */
Eo=1/(mu*clt*clt);          /* Permitivity of free space */
Er=3.90;                 /* Relative dielectric const of coax insulator */
SqtEr=Sqrt(Er);
ceff=clt/SqtEr;             /* Speed of light in the dielectric */
rho=2.62E-8;                /* Resistivity of Aluminum at 20°C in Ω-m */
// Line Dimensions and dc impedance, ZoDC (ac Zo is complex for lossy line)
Ra=1.27E-5*1.5;             /*  Center Conductor, 1.500 mil dia  */
RCENTdc=rho/(pi*Ra*Ra);       /* Coax Center Conductor resistance/meter */
Rdc=(rho/pi)*((1/(Ra*Ra))); /* Actual dc resistance as there is no shield */
LINTdc=(mu/(8*pi));         /* Lo' value for Gardiol's Eq. 4.71 incl shield */
x=1.0000;                   /*  x=1 meter interconnect line length  */
// Function Definitions
hh=0.02;                 /* Derivative step size used when these are called */
function FctI(x)
                    return bei(0,x);
end function;
function FctR(x)
                    return ber(0,x);
end function;
// Begin Actual Frequency Domain Calculation:
i=1;                     /* freq=0 dc case prior to frequency sweep  */
freq[i]=FreqStep*(i-1);
          w=2*pi*freq[i];
          RsArr[i]=Rdc;
          LintArr[i]=LINTdc;
          FRLArr[i,1]=FreqStep*(i-1);
          FRLArr[i,2]=Rdc;
          FRLArr[i,3]=LINTdc;
// Frequency Sweep:
for i=2 to NS do
           freq[i]=FreqStep*(i-1); /* Save frequency values array for use with MagY(f) plots*/
           w=2*pi*freq[i];
           // Skin effect depth delta=sqrt((2*rho)/(w*mu)); and zeta=(Ra*sqrt(2.0))/delta;
           zeta=Ra*sqrt((w*mu)/rho);    /* if zeta>10, the high frequency approx is good */
           if zeta>10 then
                    Rac=Rdc*(zeta/2)*(rSqrt2+(0.5011275/(zeta-0.475))); /* Approx RacBer Fn */
                    zzz=0.5156/(zeta-0.667);   /* temporary var in numerical Approx to LintBer */
                    Lint=LINTdc*(4/zeta)*(rSqrt2-(zzz*zzz));          /* Approx to LintBer Fn */
           end if;
           if zeta <=10 then
                    BUR=ber(0,zeta);
                    BI=bei(0,zeta);
                    BURP=derivative(FctR,3,hh,zeta);
                    BIP=derivative(FctI,3,hh,zeta);
                    Rac=Rdc*(zeta/2)*((BUR*BIP)-(BI*BURP))/((BIP*BIP)+(BURP*BURP));
                    Lint=LINTdc*(4/zeta)*((BI*BIP)+(BUR*BURP))/((BIP*BIP)+(BURP*BURP));
           end if;
          LintArr[i]=Lint;
          RsArr[i]=Rac;
          FRLArr[i,1]=FreqStep*(i-1);
          FRLArr[i,2]=Rac;
          FRLArr[i,3]=Lint;
          end for;
```

FIGURE 29.

ac Resistance, Rac/l, and Internal Inductance, Lint/l, for 1.5 mil Diameter Al, Au and Cu Wires

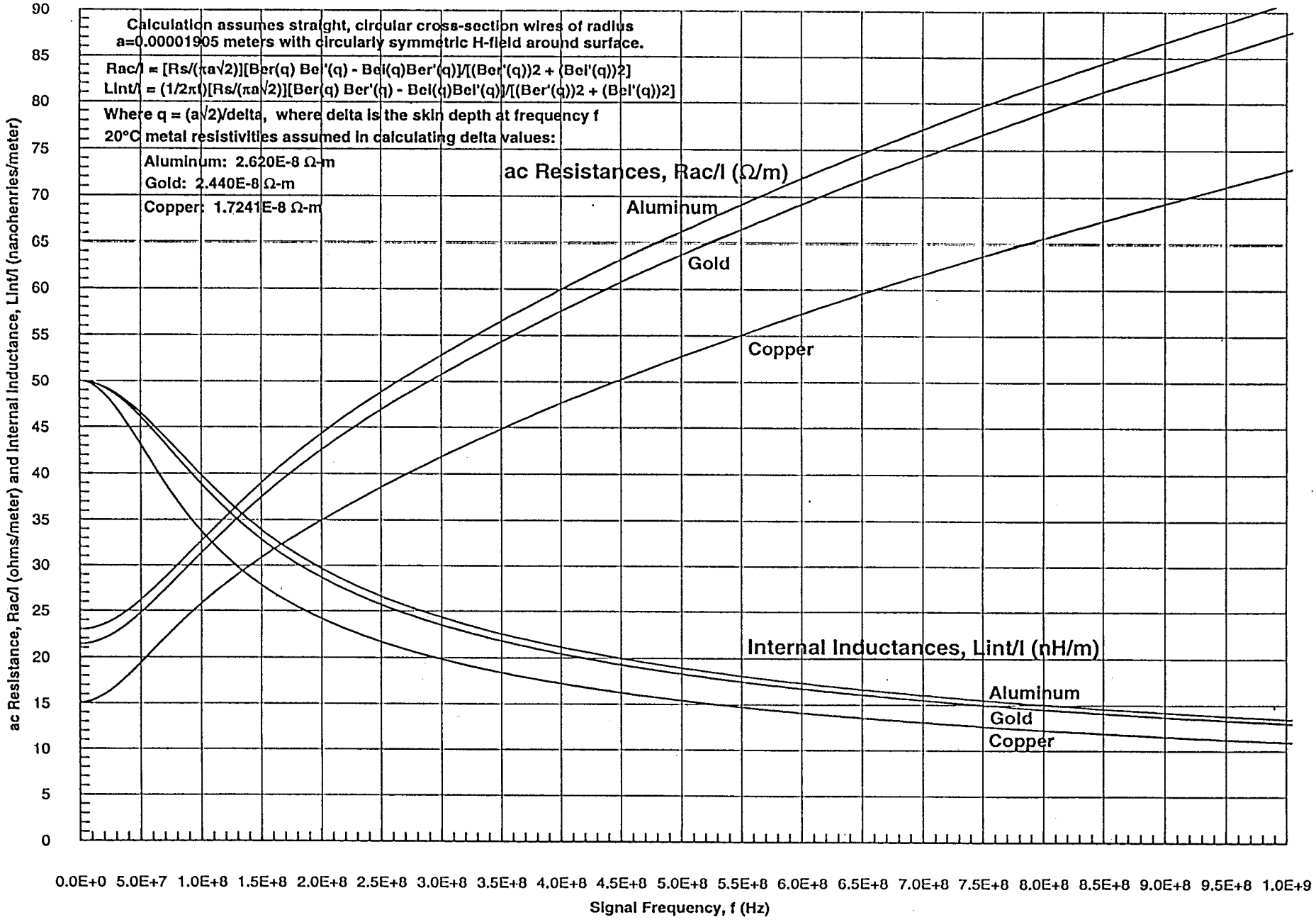
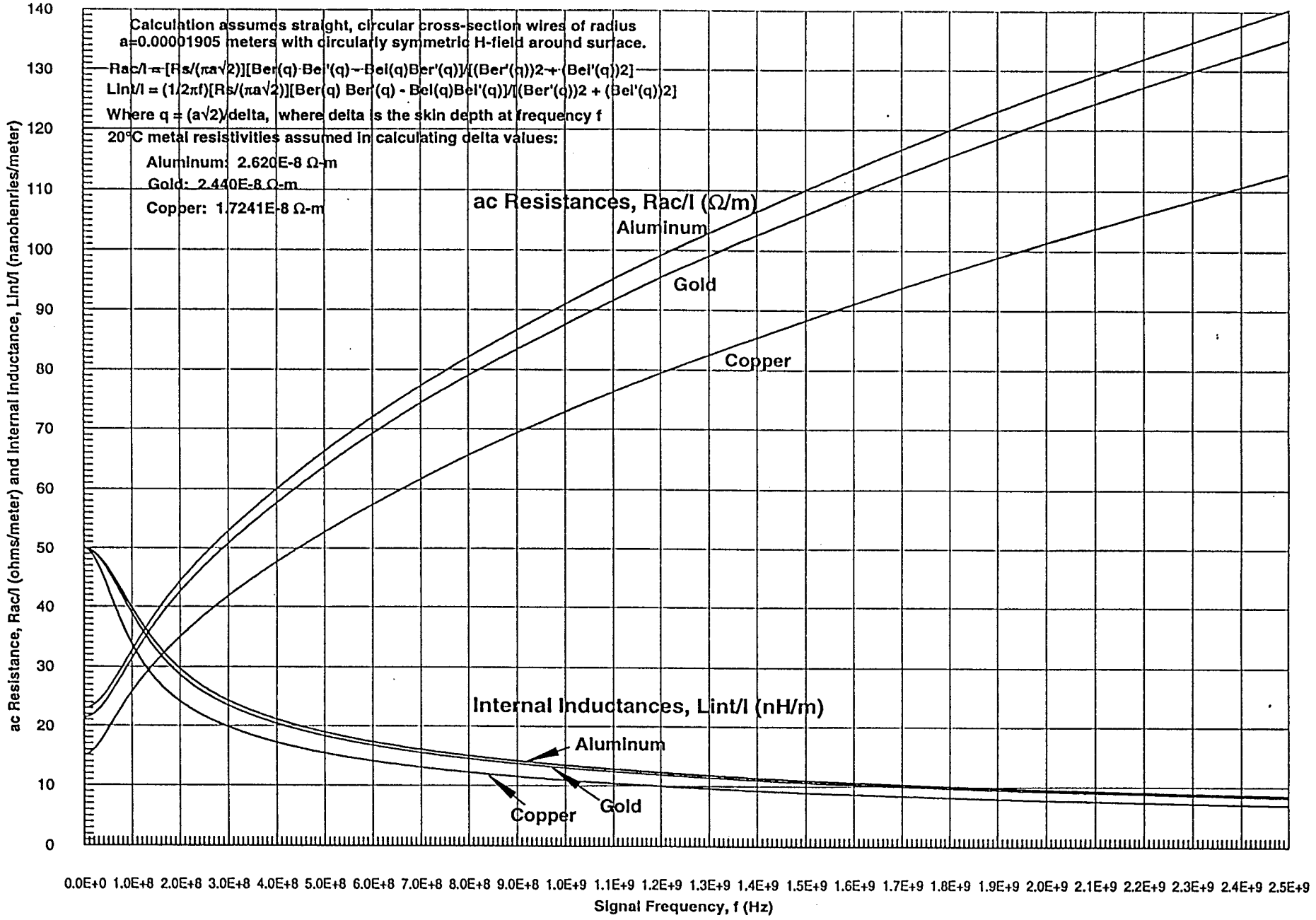


Figure 30

ac Resistance, Rac/l, and Internal Inductance, Lint/l, for 1.5 mil Diameter Al, Au and Cu Wires



ac Resistance, Rac/l, and Internal Inductance, Lint/l, for I.0 mil Diameter Al, Au and Cu Wires

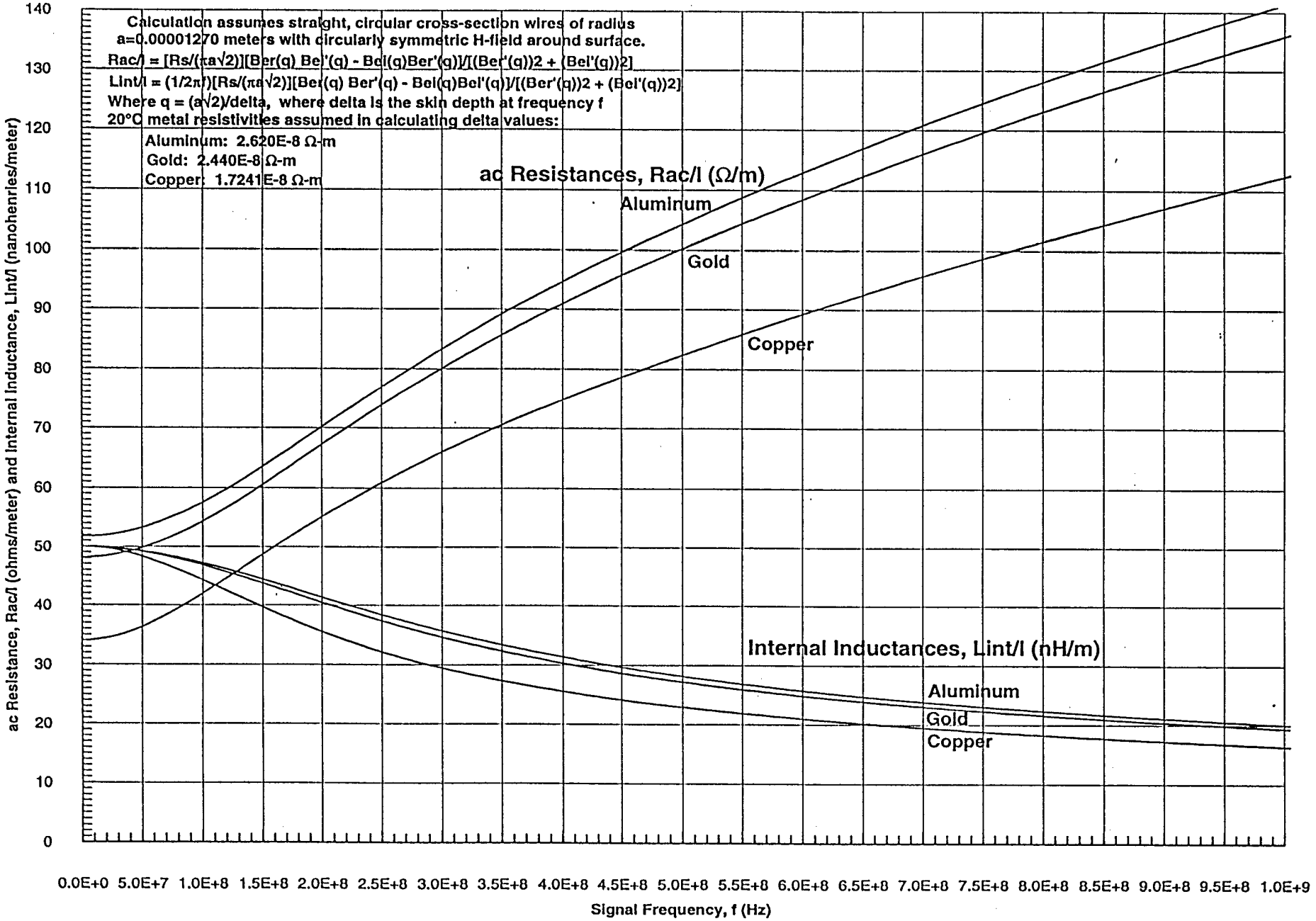


FIGURE 31a

ac Resistance, Rac/l, and Internal Inductance, Lint/l, for I.0 mil Diameter Al, Au and Cu Wires

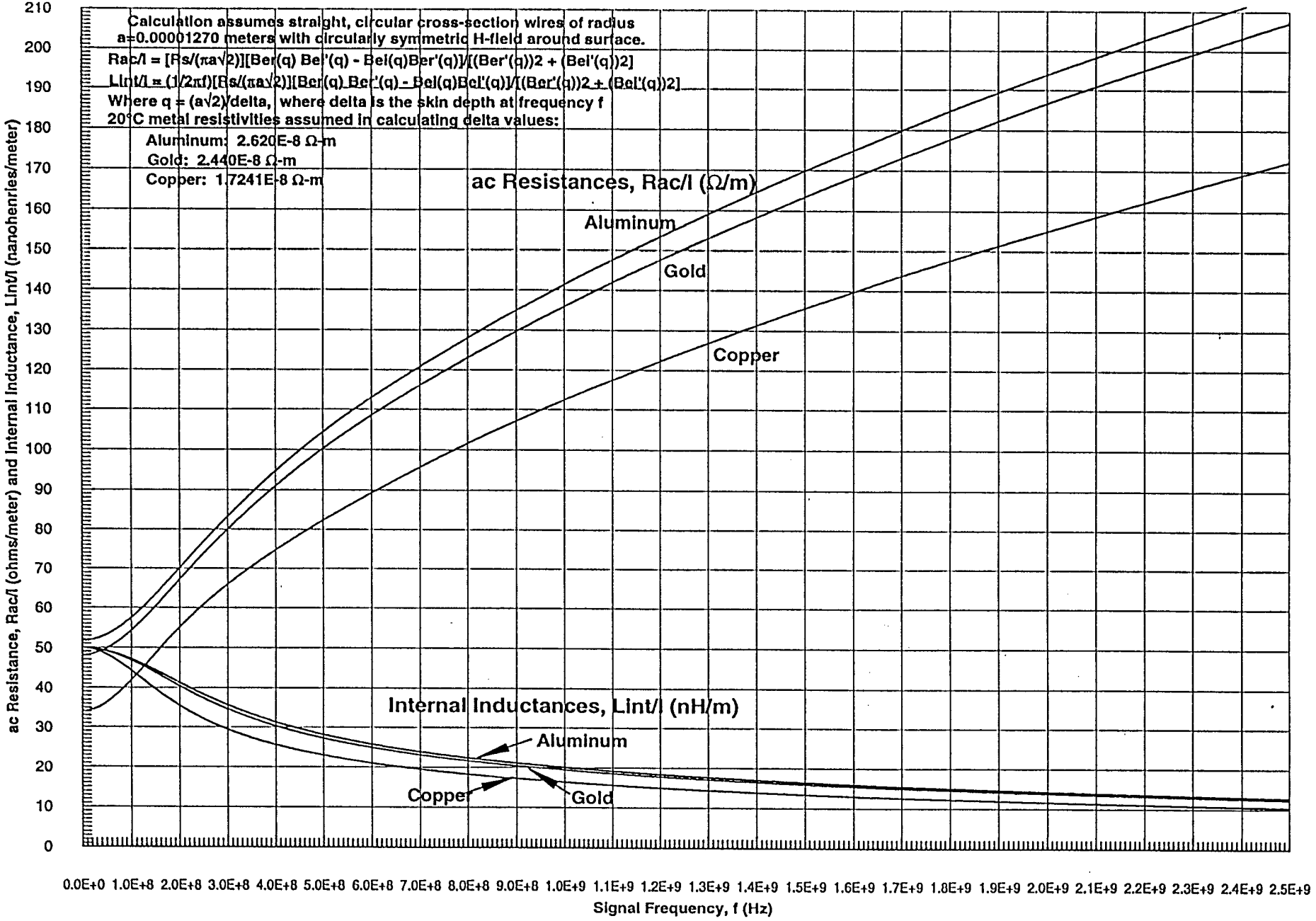


Figure 311

1.5 mil Aluminum Wire Round Coil Inductor Q vs. f for various numbers of turns, N

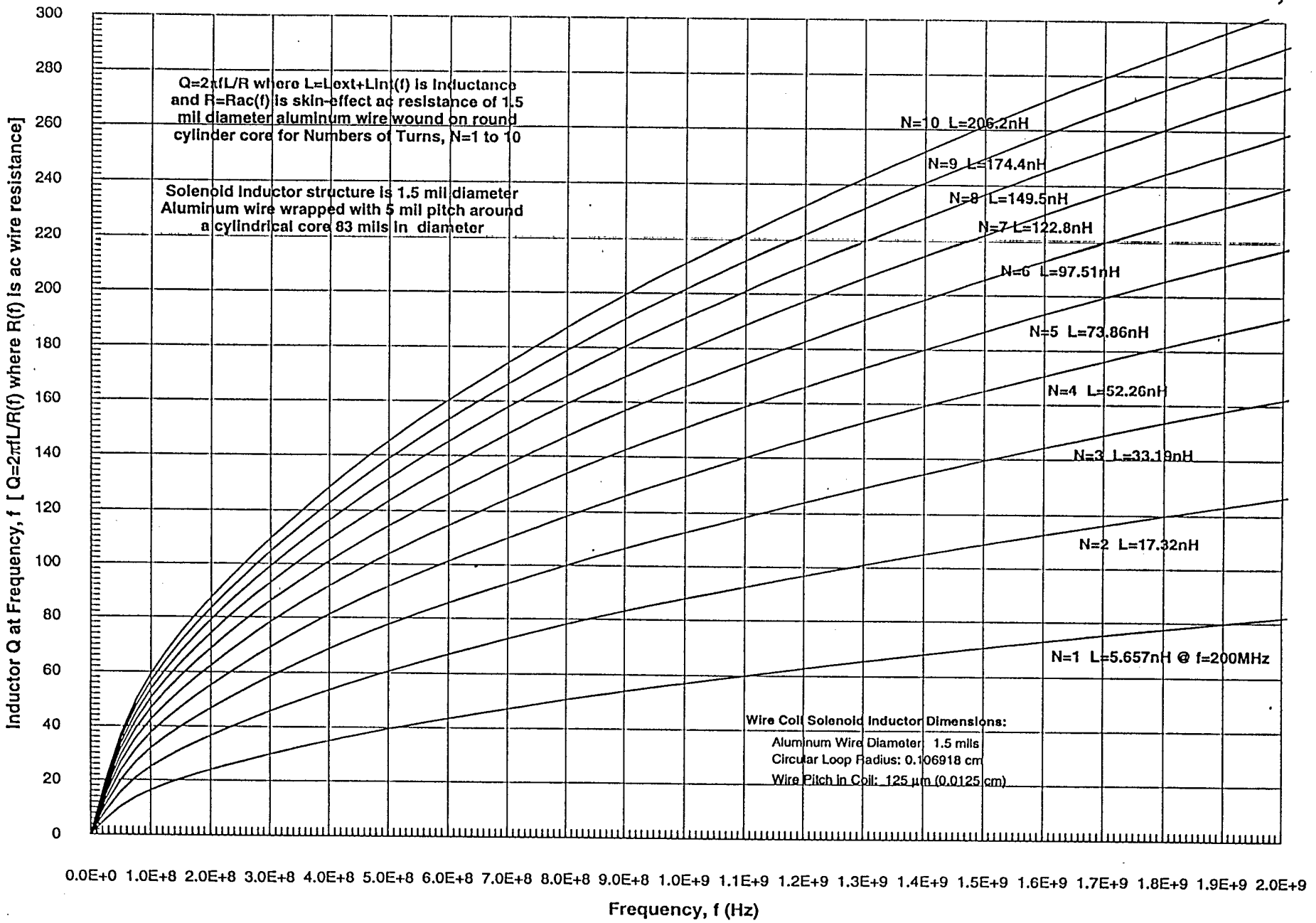


FIGURE 32.

1.0 mil Aluminum Wire Round Coil Inductor Q vs. f for various numbers of turns, N

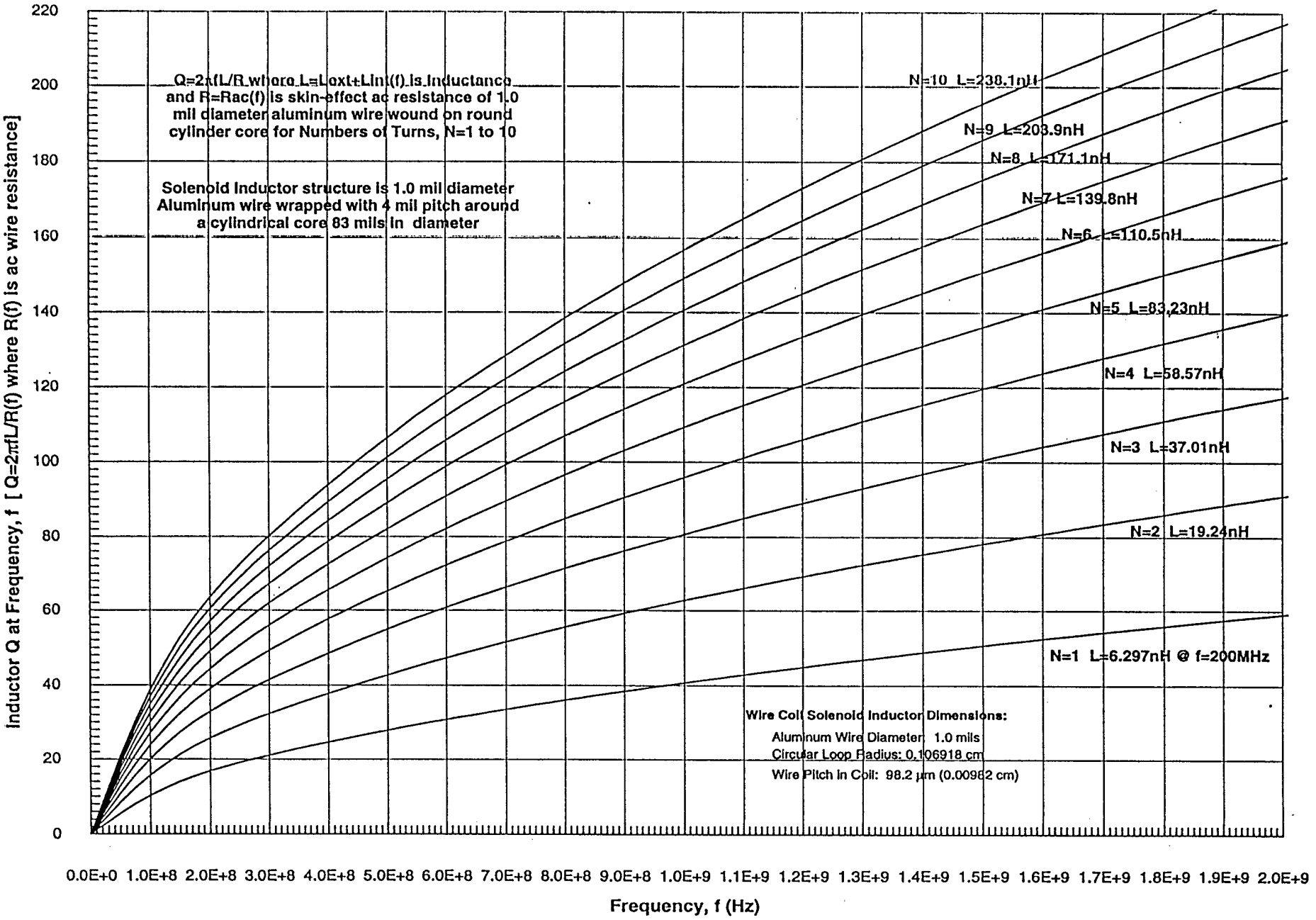


FIGURE 33.

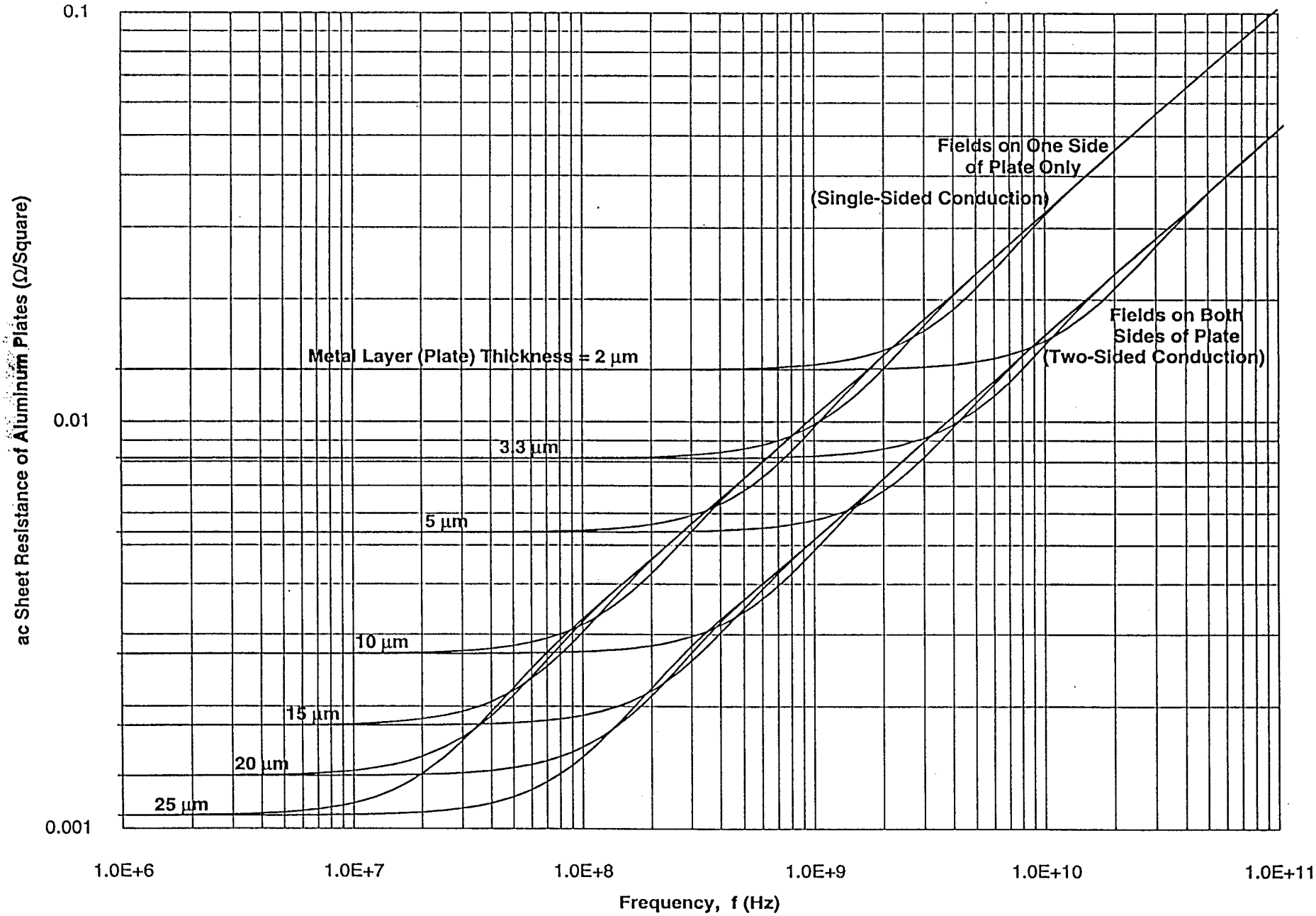

Frequency Dependence of ac Sheet Resistance of Aluminum Plates with One or Both Sides Conducting
0.1
0.01
0.001
ac Sheet Resistance of Aluminum Plates (Ω/Square)
Fields on One Side of Plate Only
(Single-Sided Conduction)
Fields on Both Sides of Plate
(Two-Sided Conduction)
Metal Layer (Plate) Thickness = 2 μm
3.3 μm
5 μm
10 μm
15 μm
20 μm
25 μm
1.0E+6
1.0E+7
1.0E+8
1.0E+9
1.0E+10
1.0E+11
Frequency, f (Hz)

FIGURE 34.

Wirebond Solenoid Inductor Structure

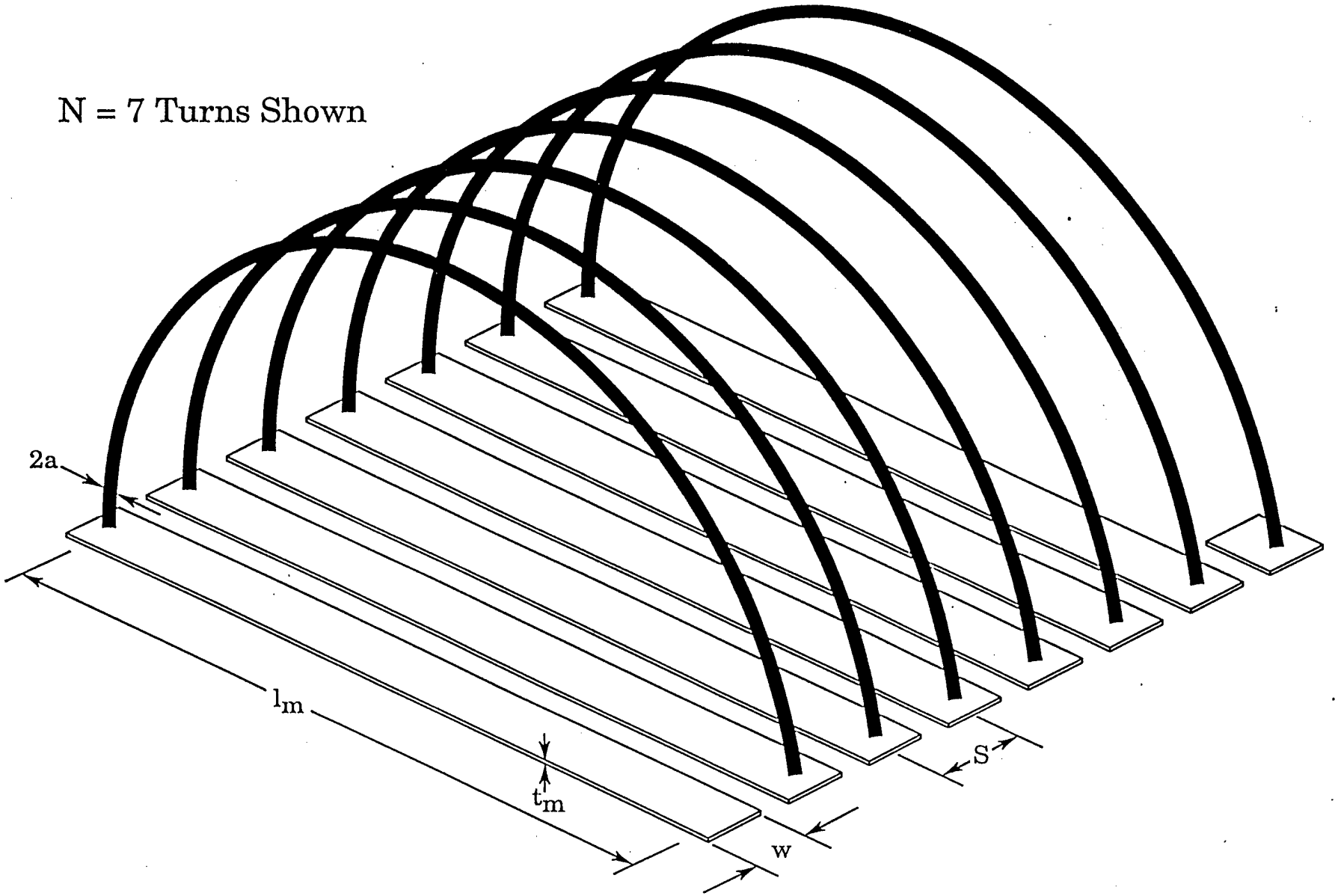
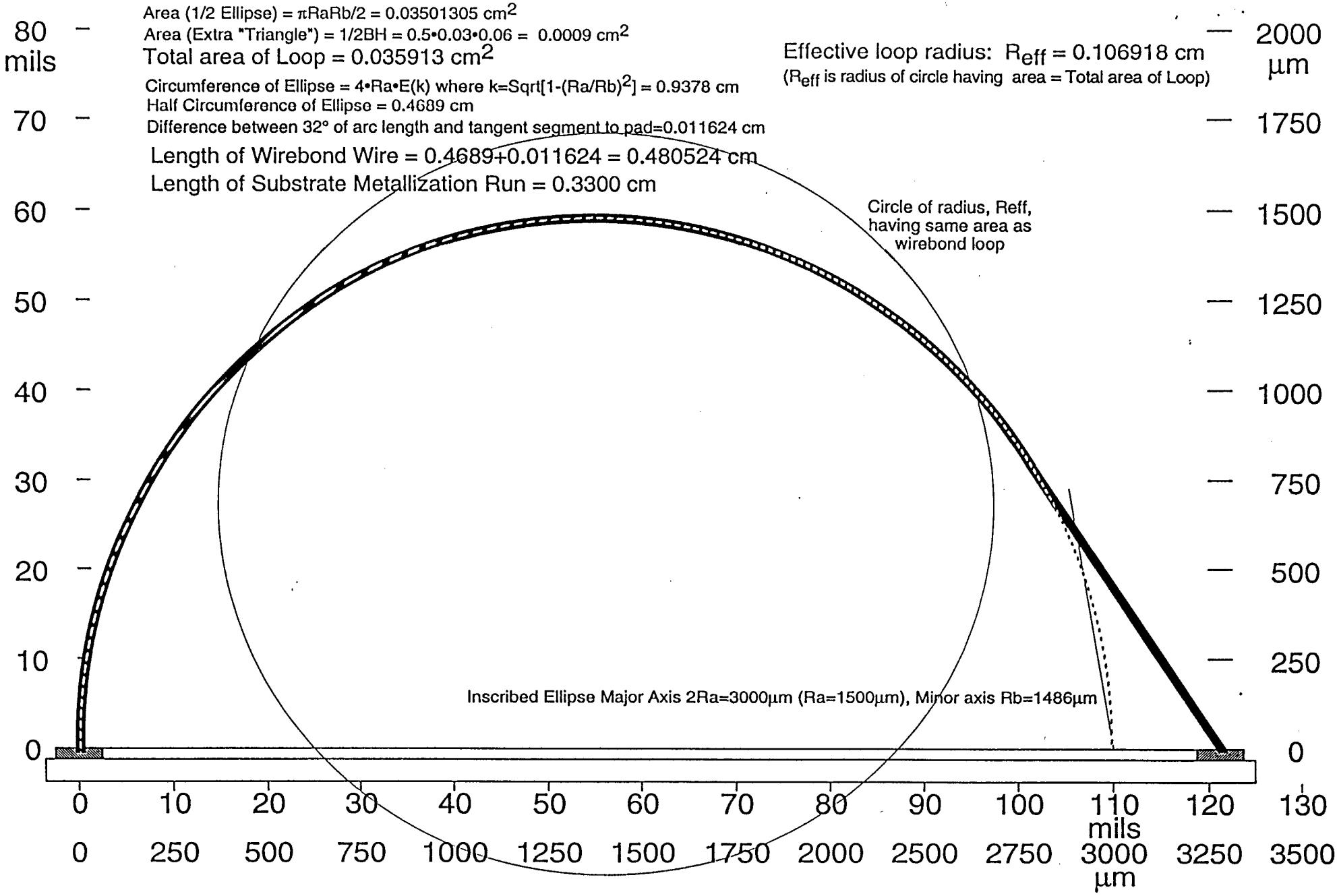


FIGURE 35.

Detailed Cross-Section Assumed for Wirebond Inductor Loop



Base=3300µm Typ (3200-3400µm), Loop Height=58.5 mils Typ (1486µm) with 58.26 to 58.79 mil range

FIGURE 36

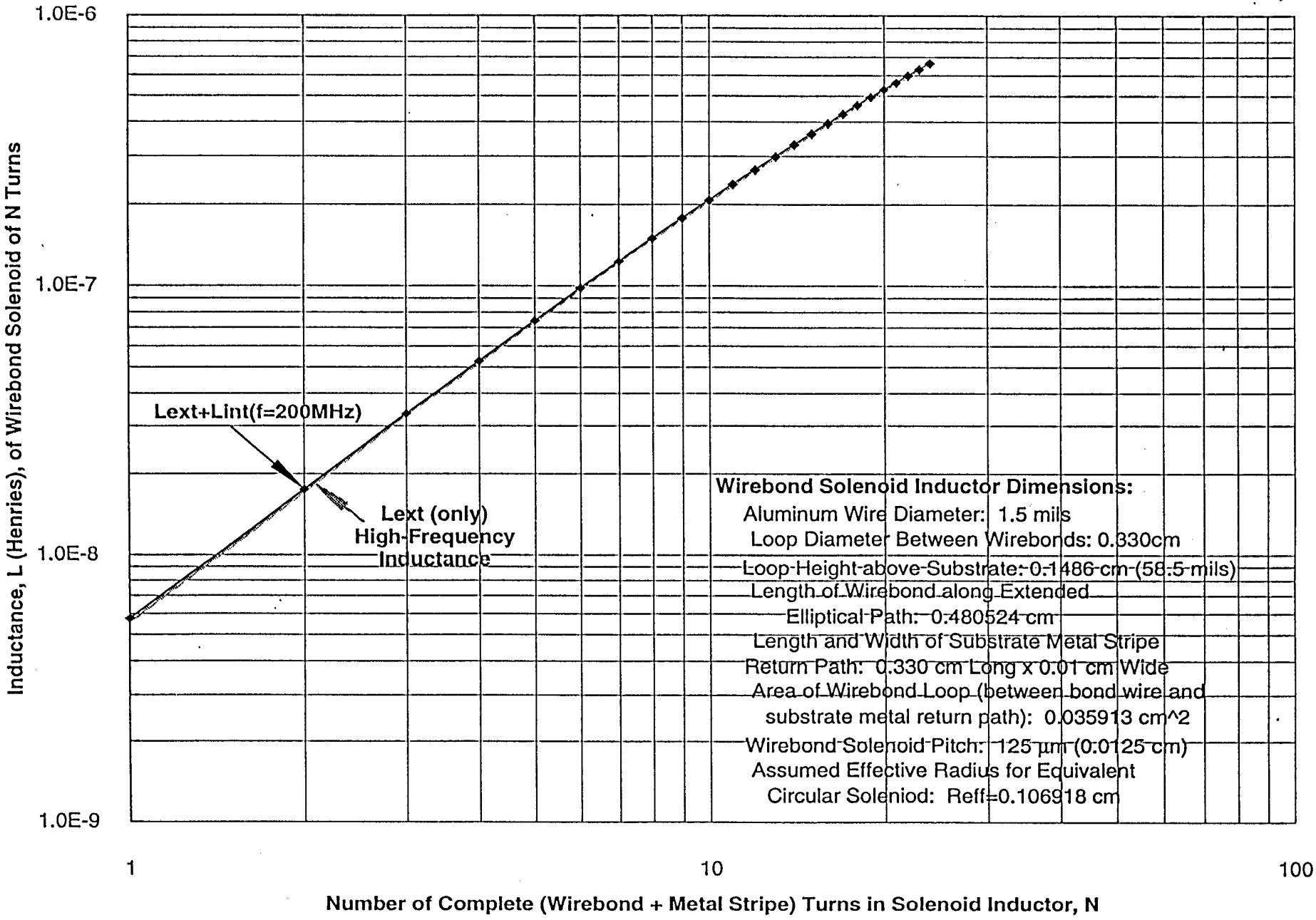

Inductance vs. Number of Turns for 1.5 mil Al Wirebond Inductor
1.0E-6
1.0E-7
1.0E-8
1.0E-9
Inductance, L (Henries), of Wirebond Solenoid of N Turns
Lext+Lint(f=200MHz)
Lext (only)
High-Frequency
Inductance
Wirebond Solenoid Inductor Dimensions:
Aluminum Wire Diameter: 1.5 mils
Loop Diameter Between Wirebonds: 0.330cm
Loop Height above Substrate: 0.1486 cm (58.5 mils)
Length of Wirebond along Extended
Elliptical Path: 0.480524 cm
Length and Width of Substrate Metal Stripe
Return Path: 0.330 cm Long x 0.01 cm Wide
Area of Wirebond Loop (between bond wire and
substrate metal return path): 0.035913 cm^2
Wirebond Solenoid Pitch: 125 µm (0.0125 cm)
Assumed Effective Radius for Equivalent
Circular Soleniod: Reff=0.106918 cm
1
10
100
Number of Complete (Wirebond + Metal Stripe) Turns in Solenoid Inductor, N

FIGURE 37

MCM 1.5 mil Al Wirebond Inductor Q vs. f for various numbers of turns, N

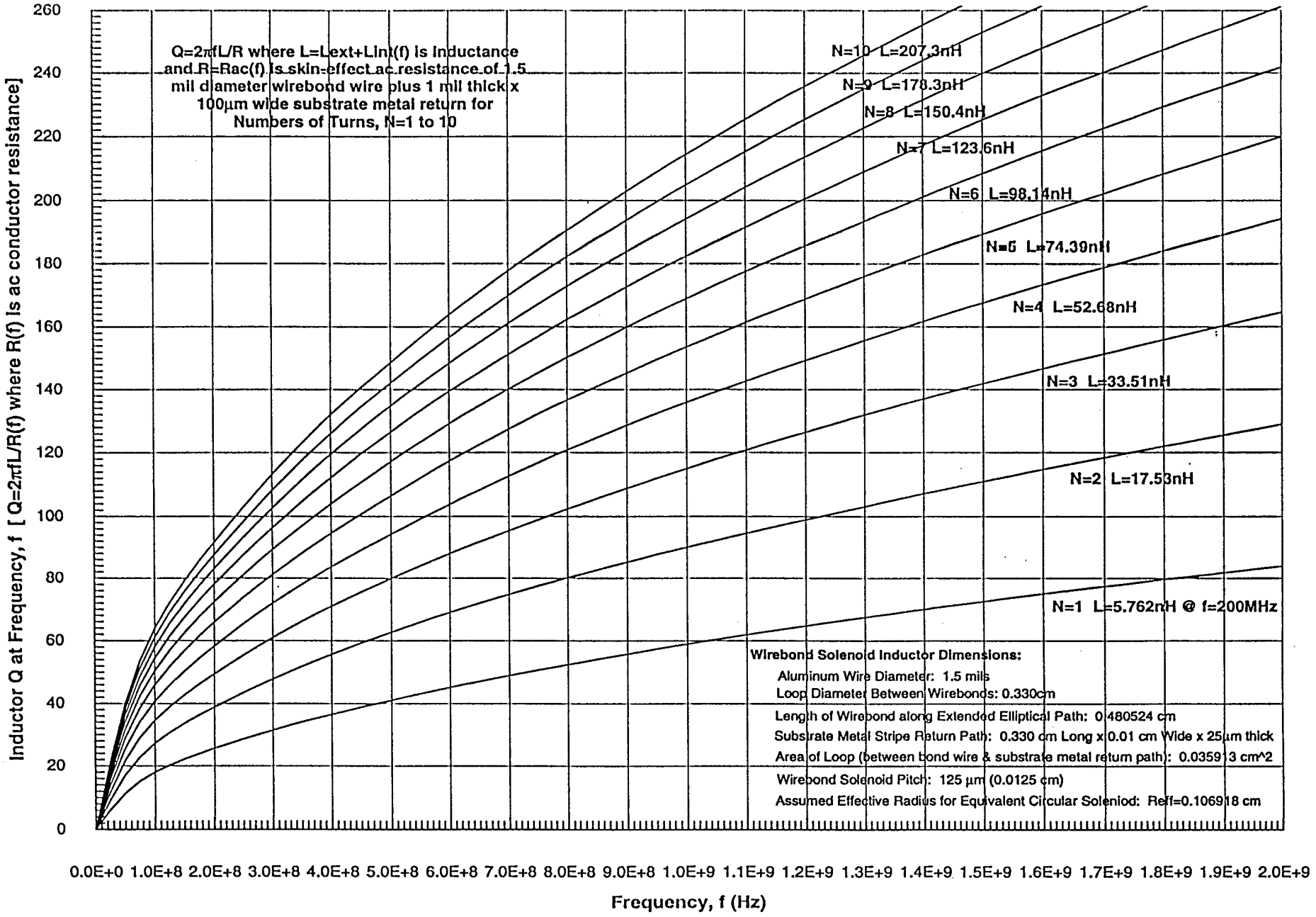
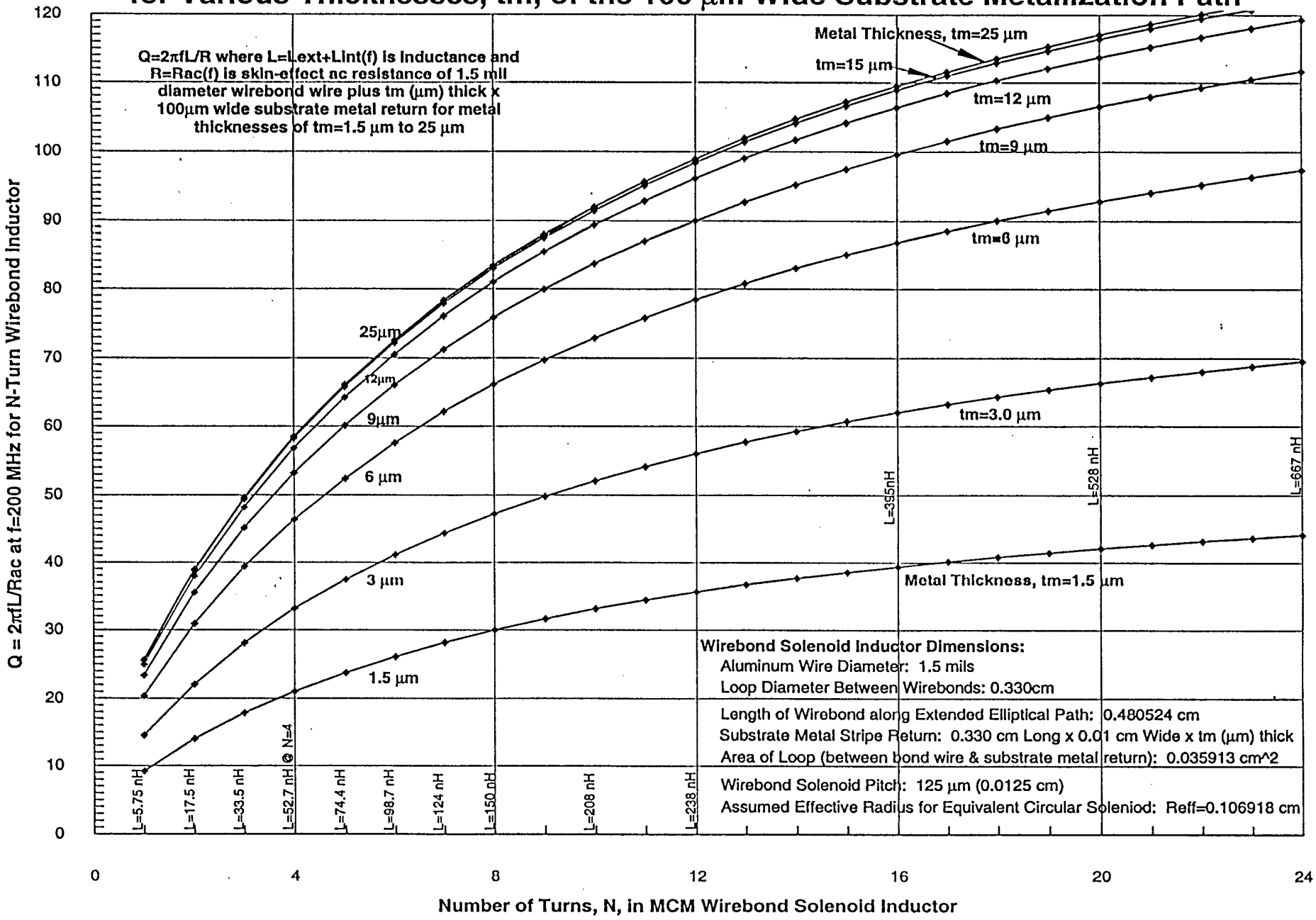


FIGURE 38

Q at f=200 MHz of 1.5 mil Al Wirebond Solenoid Inductors vs. Number of Turns, N for Various Thicknesses, tm, of the 100 μm Wide Substrate Metallization Path



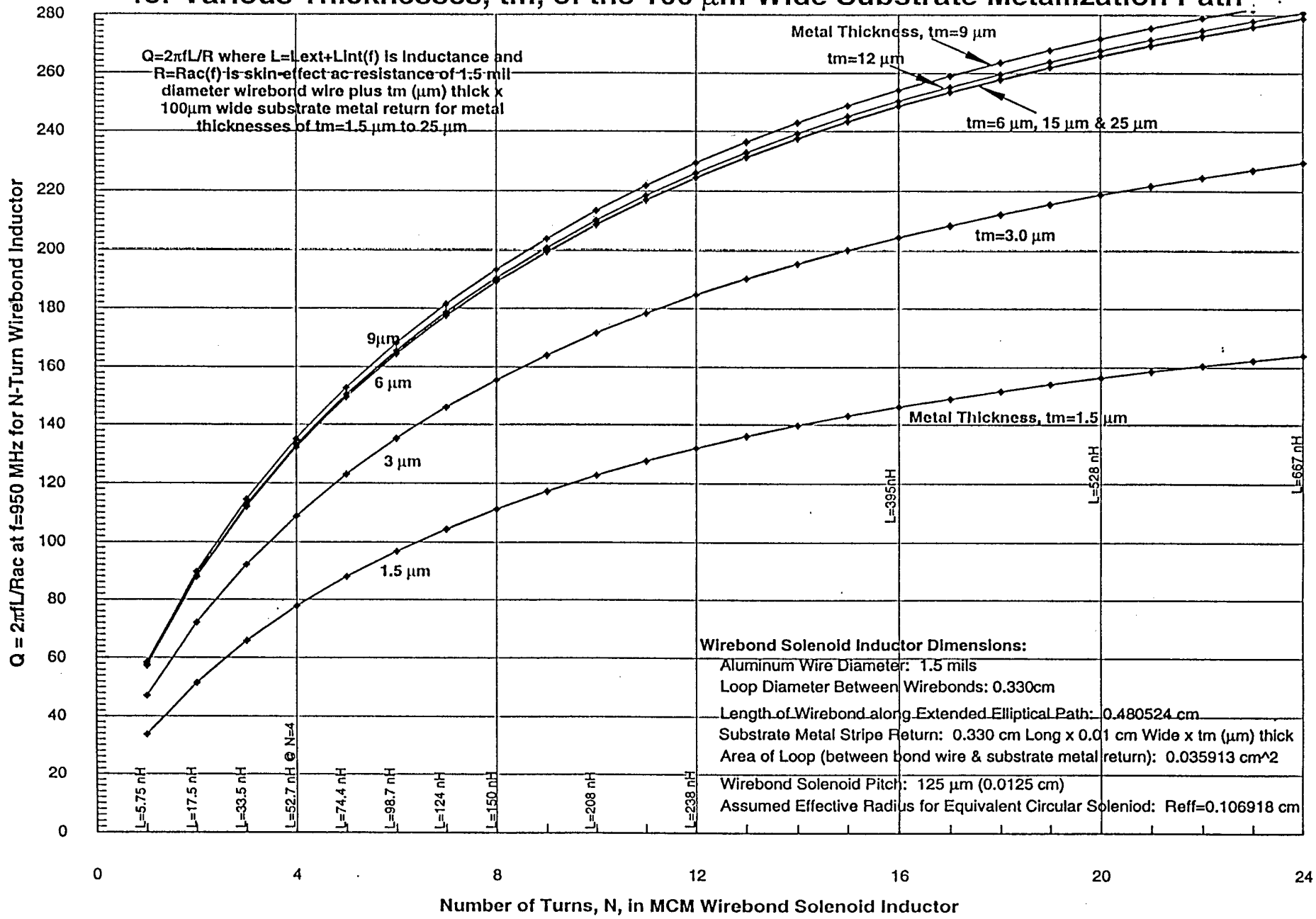

Q at f=950 MHz of 1.5 mil Al Wirebond Solenoid Inductors vs. Number of Turns, N for Various Thicknesses, tm, of the 100 μm Wide Substrate Metallization Path
Q=2πfL/R where L=LExt+LInt(f) is Inductance and R=Rac(f) is skin-effect ac resistance of 1.5 mil diameter wirebond wire plus tm (μm) thick x 100μm wide substrate metal return for metal thicknesses of tm=1.5 μm to 25 μm
Metal Thickness, tm=9 μm
tm=12 μm
tm=6 μm, 15 μm & 25 μm
tm=3.0 μm
Metal Thickness, tm=1.5 μm
9μm
6 μm
3 μm
1.5 μm
L=5.75 nH
L=17.5 nH
L=33.5 nH
L=52.7 nH @ N=4
L=74.4 nH
L=98.7 nH
L=124 nH
L=150 nH
L=208 nH
L=238 nH
L=395nH
L=528 nH
L=667 nH
Wirebond Solenoid Inductor Dimensions:
Aluminum Wire Diameter: 1.5 mils
Loop Diameter Between Wirebonds: 0.330cm
Length of Wirebond along Extended Elliptical Path: 0.480524 cm
Substrate Metal Stripe Return: 0.330 cm Long x 0.01 cm Wide x tm (μm) thick
Area of Loop (between bond wire & substrate metal return): 0.035913 cm^2
Wirebond Solenoid Pitch: 125 μm (0.0125 cm)
Assumed Effective Radius for Equivalent Circular Soleniod: Reff=0.106918 cm
Q = 2πfL/Rac at f=950 MHz for N-Turn Wirebond Inductor
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
0
4
8
12
16
20
24
Number of Turns, N, in MCM Wirebond Solenoid Inductor

FIGURE 40.

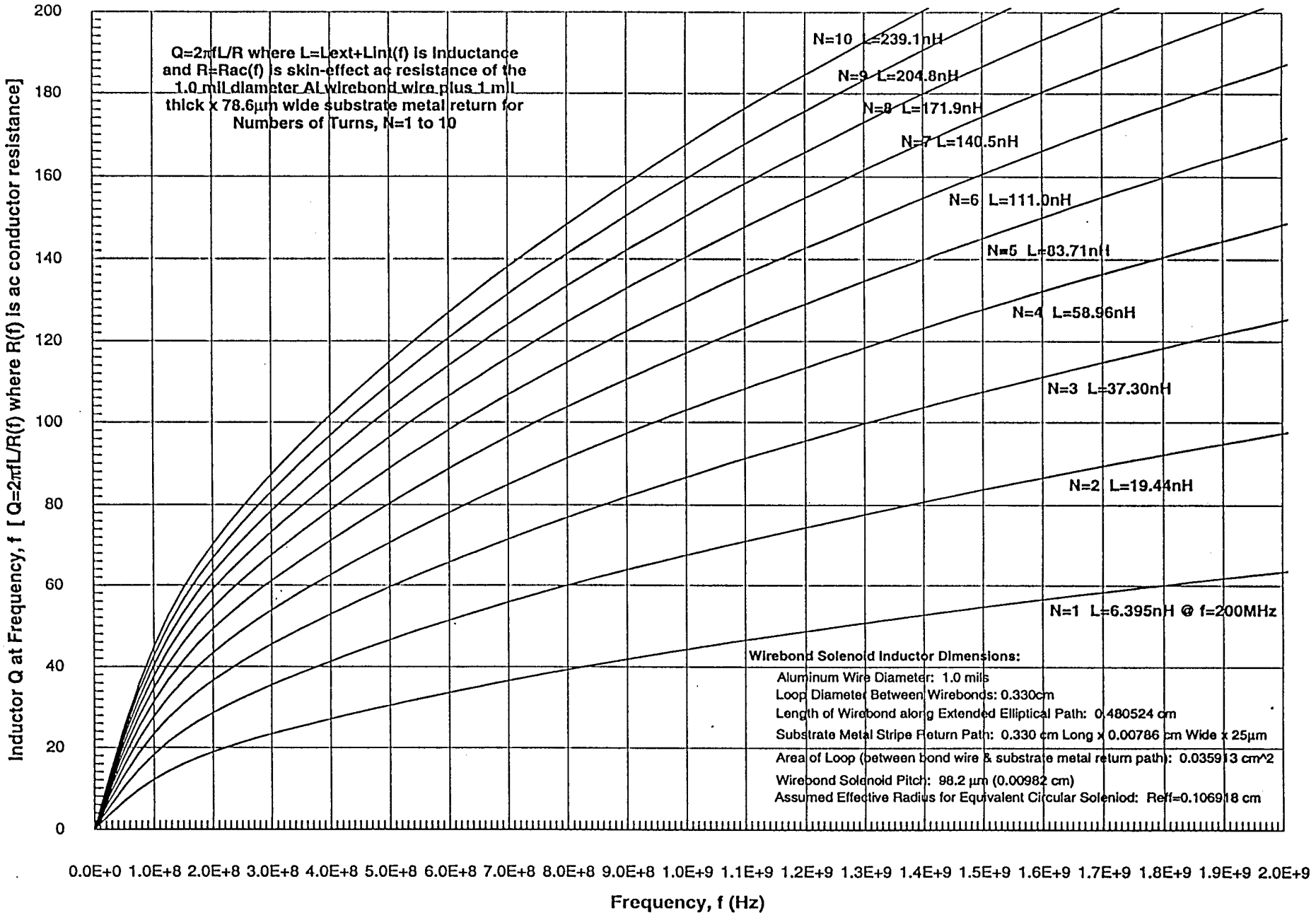
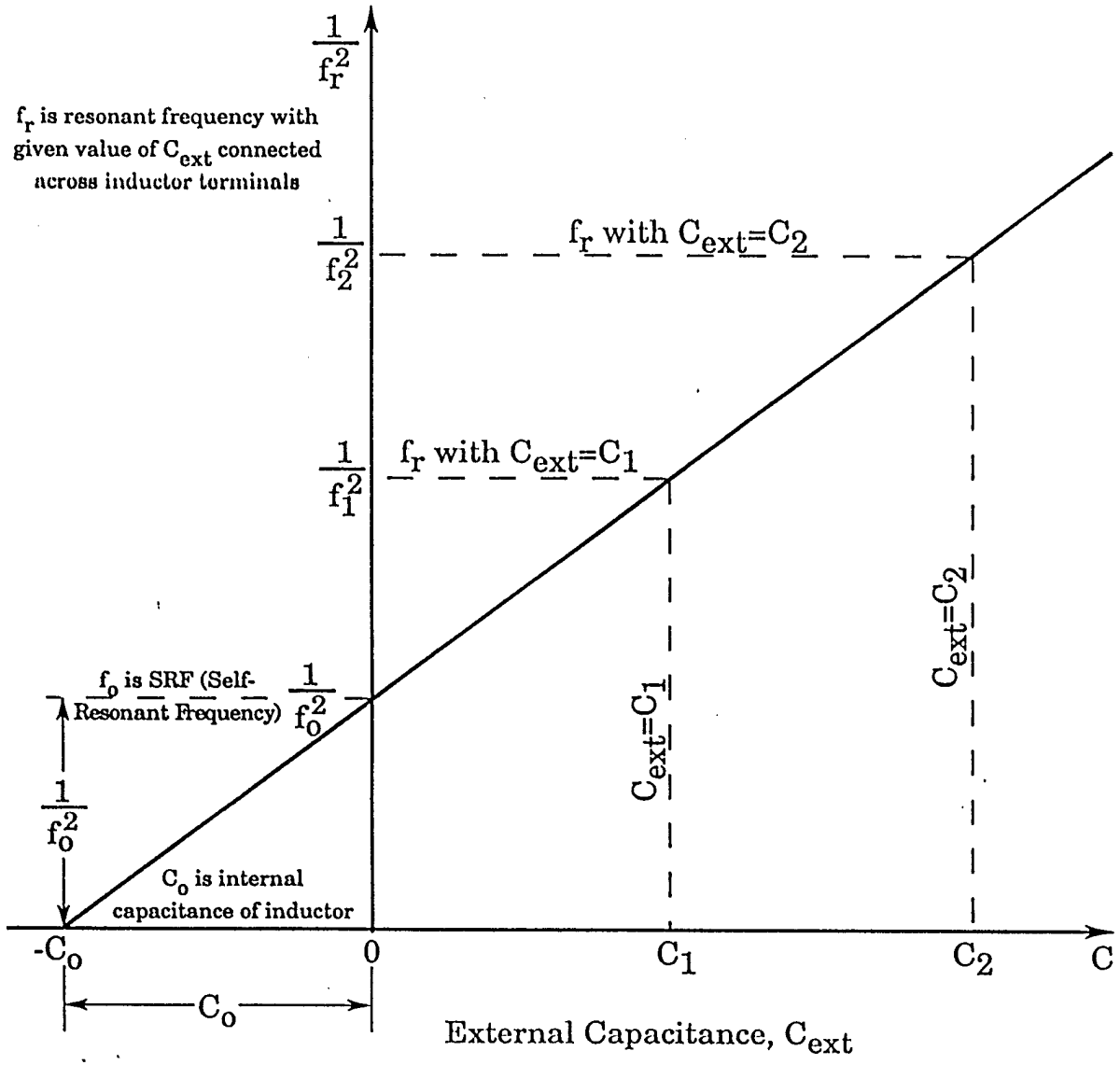

MCM 1.0 mil Al Wirebond Inductor Q vs. f for various numbers of turns, N
Q=2πfL/R where L=Lext+Lint(f) is Inductance and R=Rac(f) is skin-effect ac resistance of the 1.0 mil diameter Al wirebond wire plus 1 mil thick x 78.6µm wide substrate metal return for Numbers of Turns, N=1 to 10
N=10 L=239.1nH
N=9 L=204.8nH
N=8 L=171.9nH
N=7 L=140.5nH
N=6 L=111.0nH
N=5 L=83.71nH
N=4 L=58.96nH
N=3 L=37.30nH
N=2 L=19.44nH
N=1 L=6.395nH @ f=200MHz
Wirebond Solenoid Inductor Dimensions:
Aluminum Wire Diameter: 1.0 mils
Loop Diameter Between Wirebonds: 0.330cm
Length of Wirebond along Extended Elliptical Path: 0.480524 cm
Substrate Metal Stripe Return Path: 0.330 cm Long x 0.00786 cm Wide x 25µm
Area of Loop (between bond wire & substrate metal return path): 0.035913 cm^2
Wirebond Solenoid Pitch: 98.2 µm (0.00982 cm)
Assumed Effective Radius for Equivalent Circular Solenoid: Reff=0.106918 cm
Inductor Q at Frequency, f [Q=2πfL/R(f) where R(f) is ac conductor resistance]
0
20
40
60
80
100
120
140
160
180
200
0.0E+0 1.0E+8 2.0E+8 3.0E+8 4.0E+8 5.0E+8 6.0E+8 7.0E+8 8.0E+8 9.0E+8 1.0E+9 1.1E+9 1.2E+9 1.3E+9 1.4E+9 1.5E+9 1.6E+9 1.7E+9 1.8E+9 1.9E+9 2.0E+9
Frequency, f (Hz)

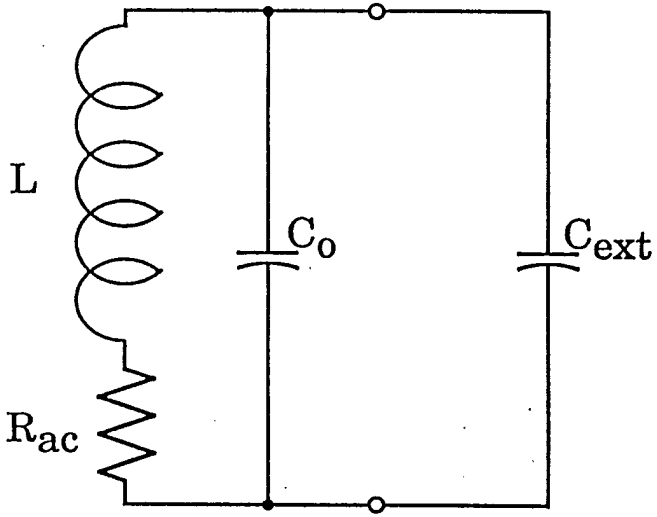
FIGURE 41.

Simplified Inductor Model and Method for Calculating True Inductance, Internal Capacitance, Self-Resonant Frequency and Q



True Inductance, L is given by:

$$L = \frac{\frac{1}{f_2^2} - \frac{1}{f_1^2}}{4\pi^2(C_2 - C_1)}$$



$$Q = 2\pi fL/R_{ac}$$

Simplified Inductor Model

FIGURE 42.